F-87
2/66

PDP-8 MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

COPY NO.

5595 PRINTED IN U.S.A. 10.0-3/66

CONTENTS

Chapter		Page
1	INTRODUCTION AND DESCRIPTION	1-1
	Computer Organization	1-2
	Processor	1-3
	Core Memory	1-4
	Input/Output	1-5
	Functional Description	1-5
	Instructions	1-6
	Major States	1-9
	Time States	1-10
	Physical Description	1-11
	Specifications	1-13
	Physical	1-13
	Electrical	1-13
	Functional	1-13
	Ambient Conditions	1-14
	Symbols and Terminology	1-14
	Digital Logic Symbols	1-14
	Conventions and Notations	1-14
	Pertinent Documents	1-17
	Abbreviations	1-18
	Reference Conventions	1-20
2	LOGICAL FUNCTIONS	2-1
	Flow Diagram Interpretation	2-1
	Prefatory Operations	2-2
	POWER and PANEL LOCK Switches	2-2
	Power Clearing	2-3
	Manual Operations	2-3
	LOAD ADD Key	2-3
	START Key	2-4
	CONT Key	2-4
	DEP Key	2-4
	EXAM Key	2-5

CONTENTS (continued)

Chapter		Page
2 (cont)	STOP Key	2-6
	SING STEP and SING INST Keys	2-6
	Programmed Operation	2-6
	Instructions	2-6
	Program Interrupt	2-19
	Automatic Operation	2-19
	Data Break	2-19
3	PROCESSOR	3-1
	Power Clear Generator (9, 16)	3-1
	Special Pulse Generator (9)	3-2
	Timing Signal Generator (9)	3-3
	Clock and TG Flip-Flop	3-4
	T1 Pulses	3-4
	T2 Pulses	3-4
	MEM START Pulse	3-5
	IOP Generator (10, 16)	3-5
	Run and Pause Control (9, 10, 16)	3-7
	Run Control (9)	3-7
	Pause Control (10)	3-8
	Instruction Register (6)	3-9
	Major State Generator (6, 10)	3-10
	Fetch State (6)	3-11
	Execute State (6)	3-11
	Defer State (6)	3-12
	Break State (6)	3-12
	Word Count State (6)	3-13
	Current Address State (6)	3-13
	Distribution of Major State Signals (6, 10)	3-13
	Program Counter Control (8)	3-14
	Clearing and Loading Operations	3-14
	Incrementing Operations	3-16
	Memory Address Register Control (8)	3-19

CONTENTS (continued)

Chapter		Page
3 (cont)	Clearing Pulses	3-19
	Loading Pulses	3-20
	Memory Buffer Register Control (5)	3-21
	Accumulator Register and Link Control (3)	3-24
	AC Command Pulses	3-24
	Link Command Pulses	3-27
	Combined AC and Link Command Pulses	3-27
	Program Counter, Memory Address, and Memory Buffer Registers (4, 8, 16)	3-29
	Program Counter Register (4)	3-29
	Memory Address Register (4)	3-30
	Memory Buffer Register (5, 16)	3-30
	Accumulator Register and Link (2, 16)	3-31
	Direct Set and Direct Clear Inputs	3-32
	DCD Jam-Transfer Inputs	3-32
	DCD Individual Set and Clear Inputs	3-32
	Complement Inputs	3-33
	Skip Control (10)	3-34
	Program Interrupt Synchronization (10)	3-35
	Type KR01 Automatic Restart Option	3-37
	Type 182 Extended Arithmetic Element	3-39
	Logical Functions	3-39
	Functional Components	3-45
	Type 681 Data Line Interface Option	3-52
	Type 680 Data Communication System Block Diagram Discussion	3-52
	Data Line Interface Logical Functions	3-53
	Data Line Interface Circuit Operations	3-55
4	CORE MEMORY	4-1
	Memory Organization	4-1
	Ferrite-Core Memory Array	4-2
	Address Selection	4-3
	Memory Selector Switches and Matrixes	4-4
	Inhibit Drivers	4-7

CONTENTS (continued)

Chapter		Page
4 (cont)	Sense Amplifiers and Master Slice Control	4-7
	Memory Control	4-7
	Detailed Circuit Operations	4-8
	Memory Selectors and Memory Selector Matrixes	4-8
	Inhibit Drivers	4-9
	Sense Amplifiers and Master Slice Control	4-9
	Memory Control	4-10
	Current Source	4-12
	Type 183 Memory Extension Control	4-14
	Block Diagram Discussion	4-15
	Circuit Operations	4-18
	Type 184 Memory Module	4-24
	Type 188 Memory Parity Option	4-24
	Logical Functions	4-24
	Circuit Operations	4-25
5	INPUT/OUTPUT	5-1
	Teletype Model 33 Automatic Send Receive Set	5-2
	Teletype Control (18)	5-2
	Type 189 Analog-to-Digital Converter (189-0-2)	5-5
	Special Input/Output Device Modules	5-11
	Type W103 Device Selector	5-11
	Type R123 Diode Gate	5-12
6	INTERFACE	6-1
	Loading and Driving Considerations	6-2
	Programmed Transfer Interface	6-3
	Accumulator Data Input (2)	6-7
	Clear AC Input (3)	6-7
	Program Interrupt Request Input (10)	6-7
	Input/Output Skip Input Connection (10)	6-7
	Buffered AC Data Output (16)	6-8
	Buffered MB Select Code Output (16)	6-8

CONTENTS (continued)

Chapter		Page
6 (cont)	IOP Generator Output (16)	6-8
	Data Break Interface	6-8
	Data Address Inputs (4)	6-13
	Data Bit Inputs (5)	6-13
	Data Break Request Input Signal (6)	6-13
	Transfer Direction Input Signal (5)	6-13
	Increment MB Input Signal (5)	6-14
	Cycle Select Input Signal (6)	6-14
	Increment CA Input Signal (5)	6-14
	Buffered MB Data Output (16)	6-14
	Buffered Break State Output Signal (10)	6-15
	Address Accepted Output (10)	6-15
	WC Overflow Output Pulse (10)	6-15
	Miscellaneous Interface	6-15
	Analog Input Signal	6-15
	LINE (1) Input and TT INST Output Signals	6-17
	Address Extension Inputs and Data Field Outputs	6-17
	Buffered Run Output Signal (10)	6-17
	Buffered Timing Pulses BT1 and BT2A (16)	6-17
	Buffered Power Clear Pulse Output (16)	6-18
	Device Selector	6-18
7	INSTALLATION	7-1
	Site Preparation	7-1
	Space Considerations	7-1
	Environmental Conditions	7-1
	Power Requirements	7-2
	Installation Procedure	7-5
8	OPERATION	8-1
	Controls and Indicators	8-1
	Operating Procedures	8-5
	Manual Data Storage and Modification	8-5

CONTENTS (continued)

Chapter		Page
8 (cont)	Loading Data Under Program Control	8-7
	Off-Line Teletype Operation	8-8
	Assembling Programs with PAL	8-10
	Teletype Code	8-11
	Programming	8-15
9	MAINTENANCE	9-1
	Preventive Maintenance	9-4
	Mechanical Checks	9-6
	Power Supply Checks	9-7
	Marginal Checks	9-8
	Memory Current Check	9-12
	Sense Amplifier Check	9-13
	Type 189 Analog-to-Digital Converter Maintenance	9-13
	Corrective Maintenance	9-22
	Preliminary Investigation	9-23
	System Troubleshooting	9-23
	Circuit Troubleshooting	9-27
	Validation Test	9-36
	Log Entry	9-37
10	ENGINEERING DRAWINGS	10-1
	Drawing Numbers	10-1
	Circuit Symbols	10-1
	Logic Signal Symbols	10-1
	Logic Levels	10-3
	Standard Pulses	10-4
	FLIP CHIP Standard Pulses	10-4
	Level Transitions	10-5
	Semiconductor Substitution	10-5
	S Series Modules	10-5
Appendix		
1	SIGNAL ORIGINS	A1-1
2	DIGITAL PROGRAM LIBRARY	A2-1

ILLUSTRATIONS

Figure		Page
1-1	Typical PDP-8 in Cabinet Model Configuration	xv
1-2	PDP-8 Simplified Block Diagram	1-2
1-3	Instruction Formats	1-7
1-4	PDP-8 Mounted in a Type CAB-8B DEC Computer Cabinet	1-12
2-1	IOT Diagram	2-15
2-2	Single-Cycle Data Break Input Transfer Timing	2-20
2-3	Single-Cycle Data Break Output Transfer Timing	2-21
2-4	Single-Cycle Data Break Memory Increment Timing	2-22
2-5	Three-Cycle Data Break Timing	2-23
3-1	Type 182 Extended Arithmetic Element Simplified Block Diagram	3-40
3-2	Type 680 Data Communications System Block Diagram	3-52
4-1	Core Memory System Block Diagram	4-1
4-2	Simple Core Memory Plane, Showing Read/Write Sense, and Inhibit Windings	4-3
4-3	Direct and Indirect Address Selection, Simplified Flow Chart	4-5
4-4	Read/Write Current Generation and Flow Path	4-6
4-5	Memory Timing Diagram	4-11
4-6	Extended Memory, Basic Block Diagram	4-14
4-7	Memory Extension Control, Block Diagram	4-16
5-1	Type W103 Device Selector Module Logic Diagram	5-12
5-2	Type R123 Diode Gate Module Logic Diagram	5-13
7-1	Table-Mounted PDP-8 Installation Dimensions	7-2
7-2	Cabinet-Mounted PDP-8 Installation Dimensions	7-3
7-3	PDP-8 Optional Cabinet and Table Installation Dimensions	7-4
8-1	PDP-8 Operator Console	8-1
8-2	Teletype Model 33-ASR Console	8-6
9-1	Power Supply Control Panel	9-3
9-2	Marginal Check Switches (Memory Panel at Top and Processor Panel at Bottom)	9-5
10-1	DEC Symbols	10-2
10-2	Standard Negative Pulse	10-4
10-3	FLIP CHIP R- and S-Series Pulses	10-4

TABLES

Table		Page
2-1	Example of Register Contents During a JMS Instruction	2-13
3-1	Automatic Restart Option Interface with Processor	3-37
5-1	Teletype Control Interface with Processor	5-3
5-2	Analog-to-Digital Converter Interface with Processor	5-6
5-3	Analog-to-Digital Converter Type 189 Characteristics	5-8
6-1	Programmed Transfer Input Interface	6-4
6-2	Programmed Transfer Output Interface	6-5
6-3	Data Break Input Interface	6-9
6-4	Data Break Output Interface	6-11
6-5	Miscellaneous Input Interface	6-16
6-6	Miscellaneous Output Interface	6-16
8-1	Operator Console Controls and Indicators	8-2
8-2	Teletype Controls and Indicators	8-4
8-3	Readin Mode Loader Program	8-7
8-4	Teletype Code	8-12
9-1	Maintenance Equipment	9-1
9-2	Maintenance Controls and Indicators	9-3
9-3	Type 708 Power Supply Outputs	9-7
9-4	Marginal Test Programs	9-11
9-5	Analog-Digital Number Conversion	9-16
9-6	Digital-to-Analog Converter Adjustment Program	9-19
9-7	Spare Parts for Printed Keyboard-Model ASR-33	9-32
9-8	Teletype Maintenance Tools	9-32
9-9	Module List	9-33
9-10	Suggested Spare Module Components	9-35
9-11	Miscellaneous Spare Parts	9-36
10-1	Semiconductor Substitution	10-5

ENGINEERING DRAWINGS

Drawing		Page
	Basic PDP-8 Power Supply Components	
RS-B-G808	Control for 708 Power Supply	10-7
RS-B-G809	−15v Sense and Relay Driver	10-7

ENGINEERING DRAWINGS (continued)

Drawing		Page
RS-C-708	Power Supply 708	10-8
	Modules	
RS-B-G007	Sense Amplifier	10-9
RS-B-G008	Master Slice Control	10-9
RS-B-G208	Inhibit Driver	10-10
RS-C-G209	Memory Selector	10-11
RS-B-G603	Memory Selector Matrix	10-12
RS-B-R002	Diode Cluster	10-12
RS-B-R113	Diode Gate	10-13
RS-B-R121	NAND Gate	10-13
RS-B-R123	Diode Gate	10-14
RS-D-R210	PDP-8 Accumulator	10-15
RS-D-R211	MA, MB, PC	10-17
RS-C-R212	MQ Register	10-19
RS-C-R220	3-Bit Shift Register	10-20
RS-B-S107	Inverter	10-21
RS-B-S111	Diode Gate	10-21
RS-B-S151	Binary-to-Octal Decoder	10-22
RS-B-S181	DC Carry Chain	10-22
RS-B-S202	Dual Flip-Flop	10-23
RS-B-S203	Triple Flip-Flop	10-23
RS-B-S205	Dual Flip-Flop	10-24
RS-C-S284	Quadraflop	10-25
RS-B-S602	Pulse Amplifier	10-26
RS-B-S603	Pulse Amplifier	10-26
RS-B-W070	Teletype Connector	10-27
RS-B-W300	Delay Line	10-27
	Basic PDP-8 Logic Elements	
BS-D-8P-0-2	Accumulator and Link	10-29
BS-D-8P-0-3	AC Control	10-31

ENGINEERING DRAWINGS (continued)

Drawing		Page
BS-D-8P-0-4	PC and MA Registers	10-33
BS-D-8P-0-5	MB Register and Control	10-35
BS-D-8P-0-6	Major State Generator and Instruction Register	10-37
BS-D-8P-0-8	MA and PC Control	10-39
BS-D-8P-0-9	Timing, Keys, Switches, and Run Control	10-41
BS-D-8P-0-10	Input/Output Control	10-43
BS-D-8M-0-11	Teletype Control	10-45
BS-D-8M-0-12	X Axis Selection	10-47
BS-D-8M-0-13	Y Axis Selection	10-49
BS-D-8M-0-15	Sense Amps, Inhibit Drivers, and Memory Control	10-51
BS-D-8M-0-16	In/Out Buffers	10-53
BS-D-8P-0-7	Flow Diagram (Sheet 1)	10-55
BS-D-8P-0-7	Flow Diagram (Sheet 2)	10-57
	PDP-8 Wiring and Module Locations	
WD-D-8-0-14	Bus Bar for Power and Logic Wiring	10-59
UML-E-8P-0-19	Processor Utilization Module List	10-61
UML-E-8M-0-20	Memory Utilization Module List	10-63
	PDP-8 Cable Lists	
CL-A-8P-0-25	Indicator Connectors for MB Bits	10-65
CL-A-8P-0-26	Indicator Connectors for AC Bits	10-66
CL-A-8P-0-27	Indicator Connectors for MA Bits	10-67
CL-A-8P-0-28	Indicator Connectors for PC and SR Bits	10-68
CL-A-8P-0-29	Indicator Connectors for PA05	10-69
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 1)	10-70
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 2)	10-71
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 3)	10-72
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 4)	10-73
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 5)	10-74
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 6)	10-75
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 7)	10-76

ENGINEERING DRAWINGS (continued)

Drawing		Page
CL-A-8P-0-31	Indicator Connectors for MQ and SR Bits	10-77
CL-A-8P-0-32	Indicator Connectors for PB05	10-78
CL-A-8P-0-34	Input Mixer (Sheet 1)	10-79
CL-A-8P-0-34	Input Mixer (Sheet 2)	10-80
CL-A-8M-0-35	AC Bits and IOP's (Sheet 1)	10-81
CL-A-8M-0-35	AC Bits and IOP's (Sheet 2)	10-82
CL-A-8P-0-36	Data Address (Sheet 1)	10-83
CL-A-8P-0-36	Data Address (Sheet 2)	10-84
CL-A-8P-0-37	MB's In (Sheet 1)	10-85
CL-A-8P-0-37	MB's In (Sheet 2)	10-86
CL-A-8M-0-38	MB Bits (Sheet 1)	10-87
CL-A-8M-0-38	MB Bits (Sheet 2)	10-88
CL-A-8M-0-39	Indicator Connector MA-35	10-89
CL-A-8M-0-40	Sense Amplifiers (Sheet 1)	10-90
CL-A-8M-0-40	Sense Amplifiers (Sheet 2)	10-91
CL-A-8M-0-44	Teleprinter	10-92
	Automatic Restart Type KR01	
BS-D-KR01-0-2	Power Interrupt	10-93
	Extended Arithmetic Element Type 182	
BS-D-182-0-2	MQ and SC Registers	10-95
BS-D-182-0-3	EAC Control	10-97
FD-D-182-0-4	EAE Flow Diagram	10-99
	Memory Extension Control Type 183	
BS-D-183-0-2	MA Buffers and Start Field	10-101
BS-D-183-0-3	Memory Extension Control	10-103
	Memory Parity Type 188	
BS-D-188-0-2	Memory Parity Network and Control	10-105

ENGINEERING DRAWINGS (continued)

Drawing		Page
	Analog-to-Digital Converter Type 189	
BS-D-189-0-2	A/D Converter	10-107
	Data Line Interface Type 681	
BS-D-681-0-2	Data Line Interface	10-109
FD-D-681-0-3	Data Line Interface Flow Diagram	10-111

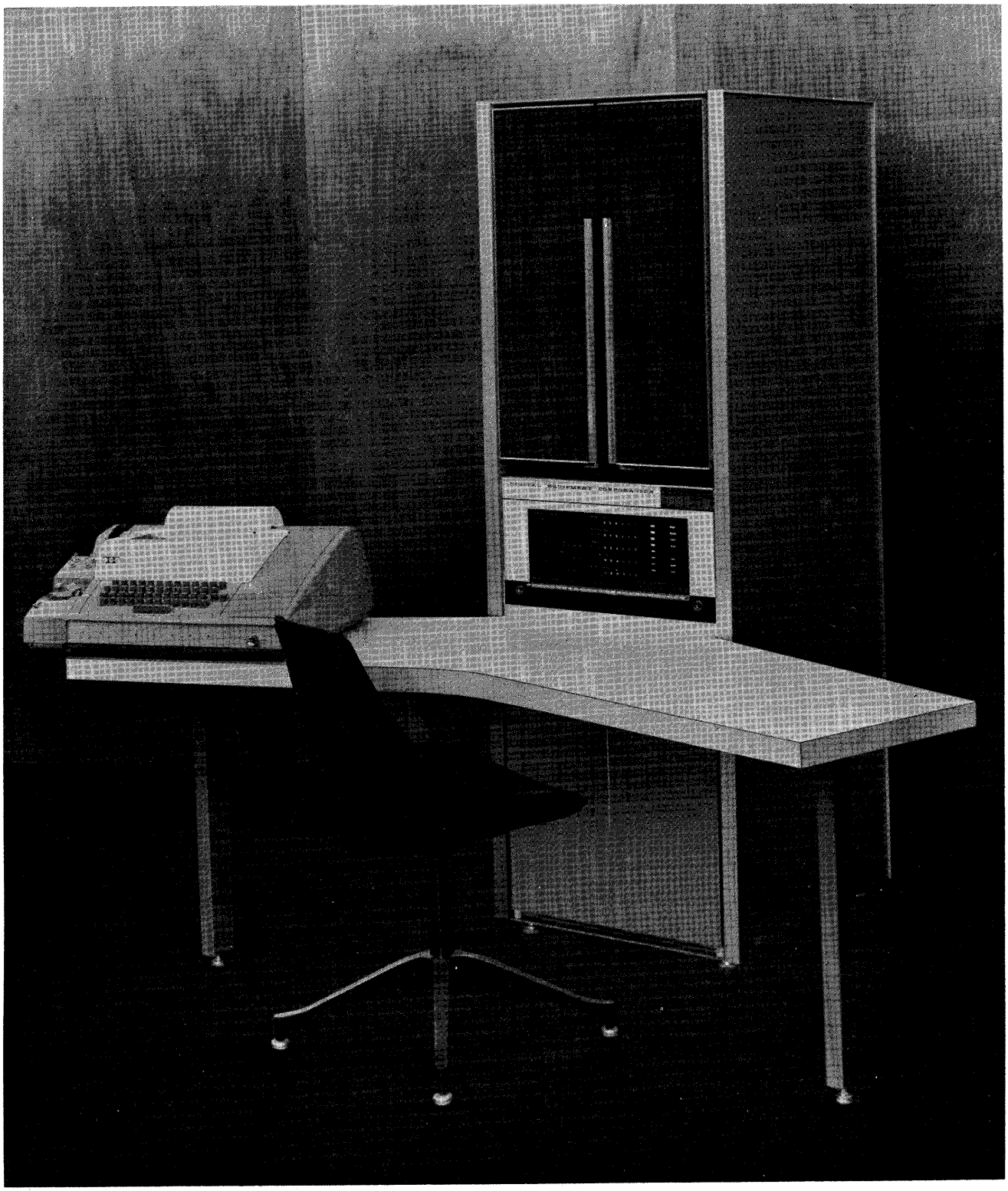


Figure 1-1 Typical PDP-8 in Cabinet Model Configuration

CHAPTER 1

INTRODUCTION AND DESCRIPTION

The Digital Equipment Corporation (DEC) Programmed Data Processor-8 (PDP-8) can serve as a small-scale general-purpose computer, as an independent information-handling facility in a large computer system, or as the control element in a complex processing system. The PDP-8 is a one-address, 12-bit fixed word length, parallel computer using 2's complement arithmetic. Cycle time of the 4096-word, random-address, magnetic-core memory is 1.5 μsec. Standard features of the system include indirect addressing, facilities for instruction skipping and program interruption as functions of input-output device conditions, and a means of transferring information with peripheral equipment via a cycle-stealing data break.

The PDP-8 performs one addition in 3.0 μsec (with one number in the accumulator), permitting a computation rate of 333,333 additions per second. It performs substraction in 6.0 μsec (with the subtrahend in the accumulator). Multiplication takes approximately 360 μsec using a subroutine that operates on two signed 12-bit numbers to produce a 24-bit product, leaving the twelve most significant bits in the accumulator. Division of two signed 12-bit numbers takes approximately 460 μsec using a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in core memory. The optional extended arithmetic element performs similar multiplication and division operations in 21 and 37 μsec, respectively.

Flexible, high-capacity, input/output capabilities of the computer allow it to operate a variety of peripheral equipment. In addition to the Teletype keyboard/printer and perforated tape reader/punch, equipment supplied with a basic PDP-8, the system can operate a number of optional devices, such as high-speed perforated tape readers and punches, card reading and punching equipment, a line printer, analog-to-digital converters, cathode-ray-tube displays, magnetic-drum systems, and magnetic-tape equipment. Instruments or equipment of special design can also be connected into the PDP-8 system. The computer needs no modification for the addition of peripheral devices.

The PDP-8 is completely self-contained, requiring no special power sources or environmental conditions. It requires a single source of 115v, 60-cps, single-phase power. Internal power supplies produce all required operating voltages. FLIP CHIP™ modules, using silicon hybrid circuits, ensure reliable operation in ambient temperatures between 32° and 130°F. Built-in provisions for marginal checking simplify and speed up preventive maintenance routines, and provide a valuable troubleshooting tool.

™FLIP CHIP is a trademark of Digital Equipment Corporation.

COMPUTER ORGANIZATION

The PDP-8 is organized into a processor, a core memory, and input/output equipment and facilities. Figure 1-2 shows the major functional elements of the PDP-8 and their signal interrelationships.

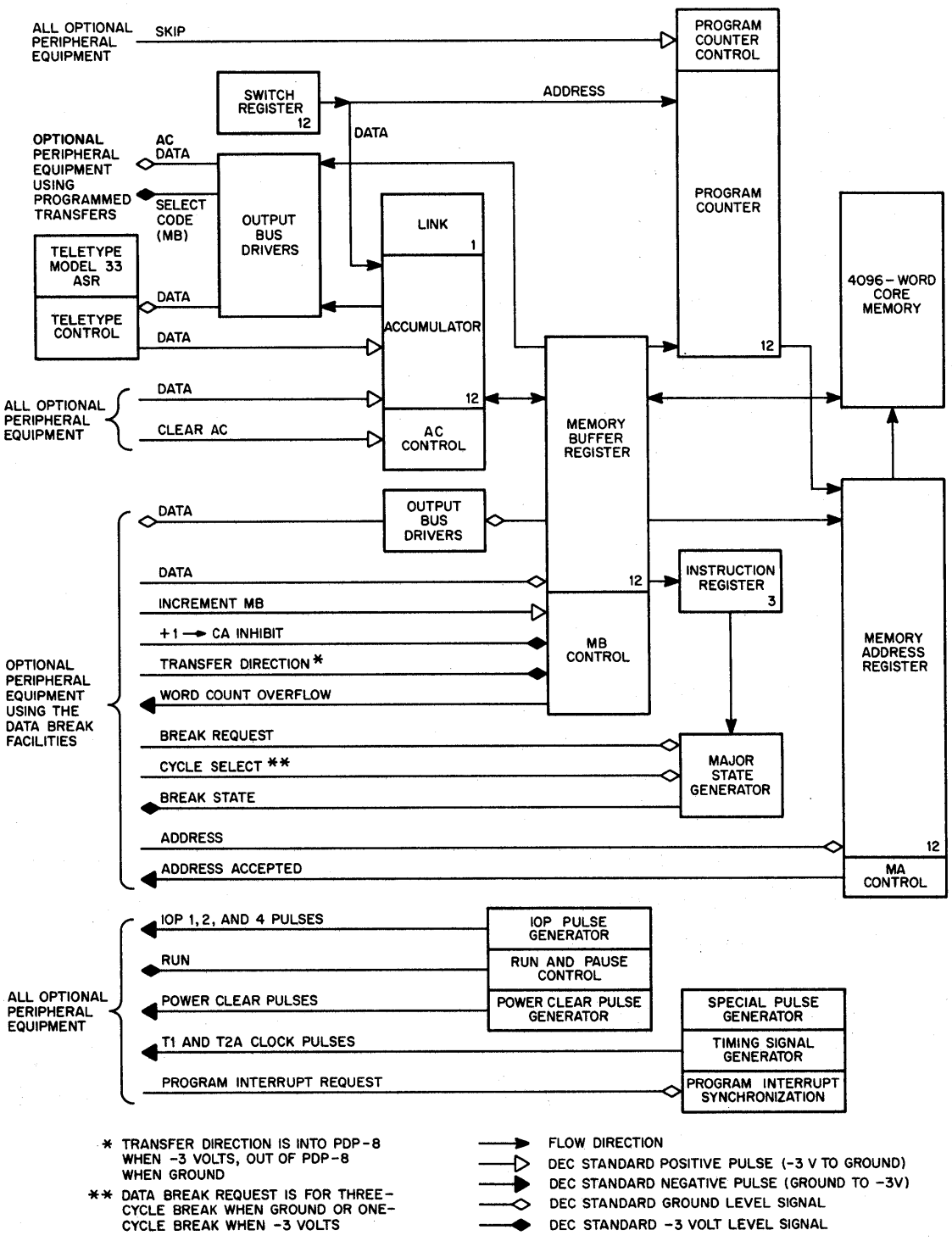


Figure 1-2 PDP-8 Simplified Block Diagram

Processor

The processor performs all arithmetic, logic, and system control operations of the standard PDP-8. The major circuit elements which perform these functions are as follows:

Accumulator (AC) - Arithmetic and logic operations occur in this 12-bit register. The AC also serves as an input/output register for programmed information transfers between core memory and peripheral equipment.

Link (L) - This 1-bit register extends the arithmetic facilities of the accumulator and serves as the carry register for 2's complement arithmetic.

Memory Buffer Register (MB) - The MB serves as a 12-bit buffer register for all information passing into or out of the core memory. The MB is a buffer directly between the core and all data registers of the processor or peripheral equipment during data break information transfers.

Memory Address Register (MA) - This 12-bit register contains the address in core memory that is currently selected for reading or writing. The MA can directly address all 4096 words of the standard core memory.

Program Counter (PC) - The PC determines the program sequence, that is, the order in which instructions are performed. This 12-bit register contains the address of the core memory location from which the next instruction will be taken.

Instruction Register (IR) - This 3-bit register contains the operation code of the instruction currently being performed by the computer. The PDP-8 loads the three most significant bits of the current instruction into the IR from the MB during a fetch cycle. It decodes the contents of the IR to produce the eight basic instructions and affect the cycles and states entered at each step in the program.

Major State Generator - The computer enters one or more major control states to determine and execute an instruction. The major state generator establishes one machine state during each computer cycle. The major states are fetch, defer, execute, word count, current address, and break. Current instruction and the current state determine the fetch, defer, and execute states. The word count, current address, and break states are entered upon receipt of the break request signal supplied by peripheral equipment.

Switch Register (SR) - Twelve toggle switches on the operator console allow manual selection of information to be set into the PC as an address, or into the AC as data to be stored in core memory.

Output Bus Drivers - Output bus driver modules which are part of the basic PDP-8 power amplify output signals from the processor. The bus drivers permit PDP-8 output signals to drive a heavy circuit load.

Timing Generators - The timing signal generator produces timing pulses used to determine the computer cycle time and to initiate sequential time-synchronized gating operations. The special pulse generator produces timing pulses used during operations resulting from the use of keys and switches on the operator console. The IOP pulse generator produces programmed timing pulses used to produce input/output transfer commands in the processor and in peripheral equipment. The power clear pulse generator produces pulses that reset registers and control circuits during power turnon and turnoff operations. Peripheral devices using programmed or data break information transfers use several of these pulses.

Control Elements - Control circuits included in the PDP-8 determine the advance of the computer program and allow instructions to be skipped as a function of conditions established in the processor or in peripheral equipment. These circuits allow peripheral equipment to interrupt a program to initiate a subroutine that performs some service for the peripheral equipment. Other control elements generate the signals that control information flow between registers within the processor.

Core Memory

The core memory provides storage for instructions to be performed and information to be processed or distributed. This random-access, magnetic-core memory holds 4096 12-bit words in the standard PDP-8. Optional equipment may extend the storage capacity in fields of 4096 words or expand the word length to 13 bits to add a parity bit to each word. Memory location 0_8 stores the contents of the PC following a program interrupt, and location 1_8 stores the first instruction to be executed following a program interrupt. Locations 10_8 through 17_8 are used for autoindexing. All other locations can store instructions or data.

The memory continuously cycles, automatically performing a read/write operation during each computer cycle. The MA and MB perform address buffering and data buffering for the core memory. The timing signal generator of the processor synchronizes operation of the memory with the processor. The major functional elements of the core memory are as follows:

Memory Selector Switches - Addresses contained in the MA are decoded to enable passage of read/write current through an X and a Y drive line of the core memory.

Diode-Balun Matrixes - Memory drivers determine the direction of read/write drive current passing through the address drive lines of the core memory.

Inhibit Selection - The MB contains data to be written into core memory. The X and Y write currents pass through the address selection lines in all bits of the addressed memory register. However, the inhibit selection circuits inhibit the setting of cores in planes which correspond to MB bits containing 0's.

Core Array - The ferrite core array consists of 12 planes that are 64 cores wide and 64 cores deep for 4096 words of memory.

Sense Amplifiers - During a read operation, sense amplifiers detect signals induced in the sense windings of the core array and convert them to standard 100-nsec pulses. These sense amplifier output pulses set corresponding bits of the MB. Thus, each read operation transfers the contents of the addressed memory cell into the MB.

Input/Output

Interface circuits for the processor allow bussed connections to a variety of peripheral equipment. Each input/output device detects its own select code and provides any necessary input or output gating. Individually programmed data transfers between the processor and peripheral equipment take place through the processor AC. The data break facilities permit data transfers to be initiated by peripheral equipment, rather than by the program. Standard features of the PDP-8 processor also allow peripheral equipment to perform certain control functions, such as instruction skipping and transfer of program control initiated by a program interrupt.

Standard peripheral equipment provided with each PDP-8 system consists of a Teletype Model 33 Automatic Send-Receive Set and Teletype control. The Teletype unit is a standard machine operating from serial 11-unit-code characters at a rate of 10 cps. The Teletype perforated tape reader or keyboard supplies input data to the computer and output data from the computer is on perforated tape and/or typed copy. The Teletype control serves as a serial-to-parallel converter for Teletype inputs to the computer and as a parallel-to-serial converter for computer output signals to the Teletype unit.

FUNCTIONAL DESCRIPTION

Keys on the operator console operate the computer on a limited scale. Operation in this manner is limited to address and data storage by the SWITCH REGISTER, core memory data examination, the normal start/stop/continue control, and the single-step or single-instruction operation that allows a program to be monitored visually as a maintenance operation.

Most of these manually initiated operations occur from executing an instruction in the same manner as by automatic programming, except special pulses rather than normal clock pulses perform the gating. In automatic operation, the program loads instructions stored in core memory into the MB and executes them during one or more computer cycles. Each instruction determines the major control states (fetch, defer, execute) that it must enter for its execution. Each control state lasts for one 1.5-μsec computer cycle

and is divided into distinct time states which can perform sequential logical operations. Gating of a specific instruction during a specific major control state at a specific time state controls any function of the computer.

Instructions

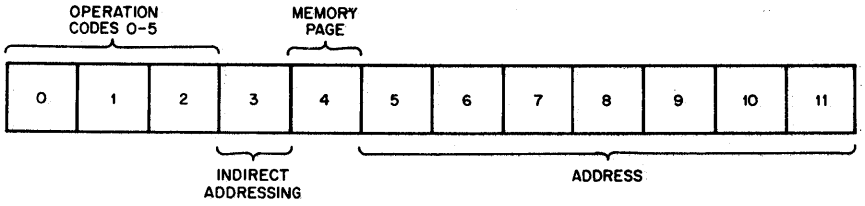
The operation code (the three most significant bits of an instruction word) goes from core memory into the IR. The IR decodes these three bits to generate the eight basic instruction signals. Memory reference instructions, designated by operation codes 0_8 through 5_8, store or retrieve data from core memory. Augmented instructions do not reference core memory and can be microprogrammed through placement of binary 1's in the remaining nine bits of the instruction to cause a variety of operations. These instructions use bits 3 through 11 to augment (or as an extension of) the operation code. Augmented instructions with an operation code of 6_8 perform input/output transfer (IOT) operations, and instructions with an operation code of 7_8 perform local data handling and control operations (OPR). Microprogramming of the IOT instruction allows combining of several bits to perform multiple operations within the limit of the capabilities of the peripheral equipment selected. Microprogramming of the operate instruction allows bit combinations and multi-function operations to be performed in two groups, as determined by the contents of bit 3 of the instruction. The format for all instruction classes appears in Figure 1-3.

Since this system can contain a 4096-word memory, twelve bits are required to address all locations. To simplify addressing, the memory is divided into blocks, or pages, of 128 words (200_8 addresses). Pages are numbered 0_8 through 37_8, a 4096-word memory using all 32 pages. The seven address bits (bits 5 through 11) of a memory reference instruction can address any location in the page on which the current instruction is located by placing a 1 in bit 4 of the instruction. By placing a 0 in bit 4 of the instruction, any location in page 0 can be addressed directly from any page of core memory. All other core memory locations must be addressed indirectly by placing a 1 in bit 3 and placing a 7-bit effective address in bits 5 through 11 of the instruction to specify the location in the current page or page 0, which contains the full 12-bit absolute address of the operand.

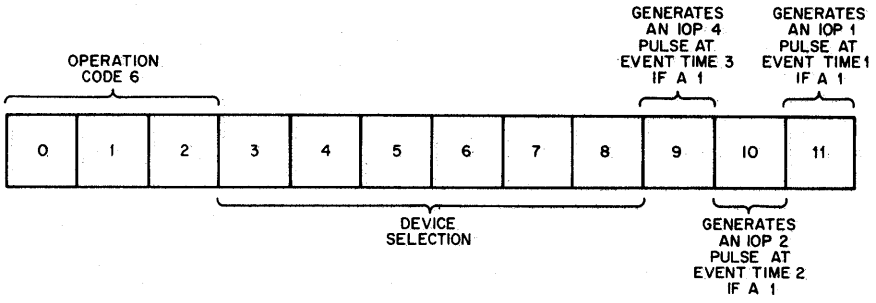
A memory reference instruction specifies a 12-bit core memory address for the operand in one of the following four ways:

1. When bits 3 and 4 of the instruction contain 0's, the operand is in page 0 at the address specified by bits 5 through 11.

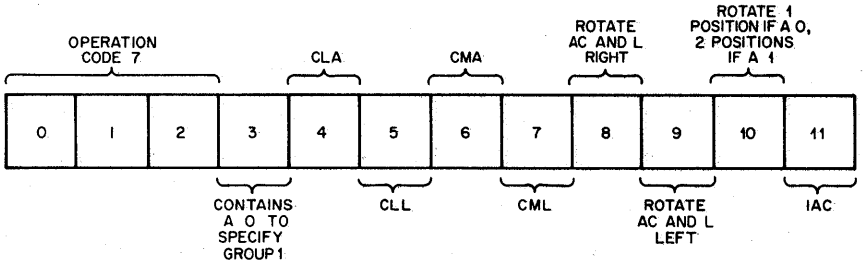
2. When bit 3 contains a 0 and bit 4 contains a 1, the operand is in the current page at the address specified by bits 5 through 11.



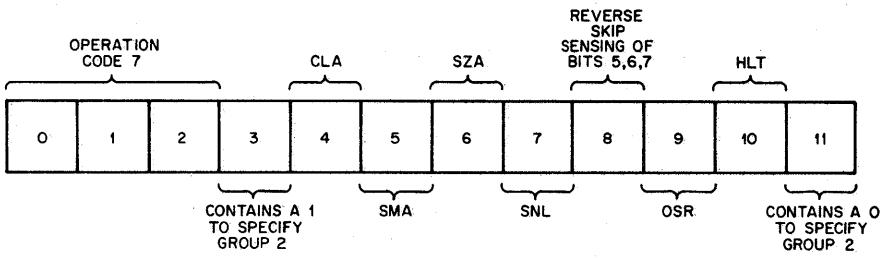
(a) Memory Reference Instruction Format



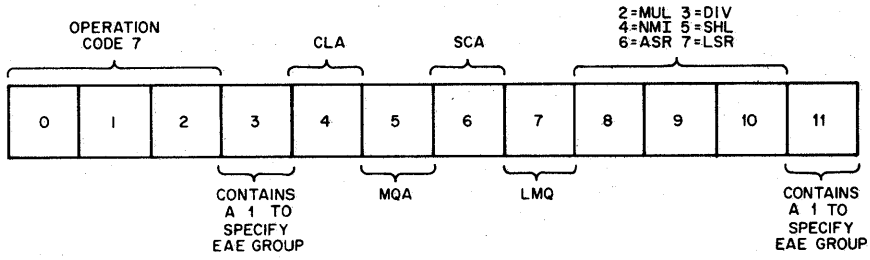
(b) IOT Instruction Format



(c) Group 1 Operate Microinstruction Format



(d) Group 2 Operate Microinstruction Format



(e) EAE Microinstruction Format

Figure 1-3 Instruction Formats

3. When bit 3 contains a 1 and bit 4 contains a 0, the absolute address of the operand is taken from the contents of the location in page 0 designated by bits 5 through 11.

4. When bits 3 and 4 both contain 1's, the absolute address of the operand is taken from the contents of the location in the current page designated by bits 5 through 11.

The memory reference instructions are:

AND (operation code 0_8) - The logical AND. The contents of the specified core memory register AND with the contents of the accumulator. The result of this combination remains in the AC, the original contents of the AC are lost, and the contents of the specified core memory location are restored.

TAD (operation code 1_8) - Two's complement add. The contents of the specified core memory location are added to the contents of the AC in 2's complement arithmetic. The result of this addition remains in the AC, the original contents of the AC are lost, and the contents of the specified core memory location are restored. If there is a carry from AC0 during this operation, it complements the link.

ISZ (operation code 2_8) - Increment and skip if 0. This operation increments by 1 the contents of the specified core memory location in 2's complement arithmetic. If the resultant contents of the specified core memory location equal 0, it increments the contents of the PC by 1, and skips the next instruction. If the resultant contents of the specified core memory location do not equal 0, the program proceeds to the next instruction. The incremented contents of the specified core memory location are restored to memory. This instruction does not affect the contents of the AC.

DCA (operation code 3_8) - Deposit and clear AC. This instruction deposits the contents of the AC in core memory at the specified core memory location, then clears the AC. The previous contents of the specified core memory location are lost.

JMS (operation code 4_8) - Jump to subroutine. JMS deposits the contents of the PC in core memory at the specified location. The program then takes the next instruction from the contents of the specified core memory address + 1. This instruction does not affect the contents of the AC.

JMP (operation code 5_8) - Jump. JMP sets the specified core memory address into the PC so that the next instruction comes from this specified core memory address. The original contents of the PC are lost. This instruction does not affect the contents of the AC.

An augmented instruction having an operation code of 6_8 is an input/output transfer (IOT) instruction. Bits 3 through 8 of an IOT instruction signify a select code for a specific I/O device or register, enabling the processor to produce IOP pulses as a result of binary 1's in bits 11, 10, and 9 of the instruction. These IOP pulses cause the selected device to produce correspondingly numbered IOT pulses that initiate operation of logic elements within the peripheral equipment and/or execute data transfers to or from the

processor. The IOP pulses occur at a specified time with respect to the computer cycle time, designated as event times 1, 2, and 3. Three event times, separated by 1 μsec, occur during the input/output transfer instruction.

Augmented instructions having an operation code of 7_8 specify the operate (OPR) instruction. Bit 3 of an OPR instruction containing a 0, indicates a group 1 (OPR1) microinstruction. Bit 3 containing a 1, indicates a group 2 (OPR2) microinstruction.

Group 1 microinstructions primarily clear, complement, rotate, and increment. Group 2 microinstructions primarily check the contents of the AC and link and continue to, or skip, the next instruction based on the check. Any logical combination of bits within one group can compare one microinstruction. Naturally, bits which cause diverse functions cannot be programmed simultaneously.

The Extended Arithmetic Element Type 182 option adds a whole class of instructions to the OPR2 instruction list. An operate instruction (operation code 7_8) in which bits 3 and 11 contain binary 1's specifies extended arithmetic element (EAE) microinstructions. Being augmented instructions, the EAE commands are microprogrammed and can be combined with each other to perform nonconflicting logical operations.

Major States

The computer enters one major state during each 1.5-μsec computer cycle. It enters fetch, defer, and execute states in succeeding cycles as required by the instruction being executed. The break state occurs upon receipt of break request signal from peripheral equipment. During this state, data transfers between the requesting device and core memory (via the MB). The word count, current address, and break states occur sequentially for a 3-cycle data break: a data break in which two core memory locations are used to record the number of words transferred and to determine the core memory address of each transfer.

Fetch (F) - During this state the program reads an instruction into the MB from the core memory location specified by the contents of the PC. It restores the instruction in core memory and retains it in the MB. The operation code of the instruction goes into the IR to cause enactment, and the contents of the PC are incremented by 1. The major state following a multiple-cycle instruction is either defer or execute. The operations specified by a one-cycle instruction occur during the last part of the fetch cycle, and the next state is another fetch.

Defer (D) - When a 1 is present in bit 3 of a memory reference instruction, the computer enters the defer state to obtain the full 12-bit address of the operand from the address in the current page or page 0, specified by bits 4 through 11 of the instruction. The process of address deferring is called indirect addressing because access to the operand is addressed indirectly, or deferred, to another memory location.

Execute (E) - The computer enters this state for all memory reference instructions except JMP. During an AND or ISZ instruction, it reads the contents of the core memory location specified by the address portion of the instruction into the MB, and performs the operation specified by bits 0 through 2 of the

instruction. A DCA instruction transfers the contents of the AC into the MB and stores them in core memory at the address specified in the instruction. During a JMS instruction, this state writes the contents of the PC into the core memory address designated by the instruction and transfers this address into the PC to change program control.

Word Count (WC) - This state is entered when an external device supplies signals requesting a data break and specifying that the break should be a 3-cycle break. When this state occurs, a transfer word count in a core memory location designated by the device is read into the MB, increments by 1, and is rewritten in the same location. If the word count overflows, indicating that the desired number of data break transfers will be enacted at completion of the current break, the computer enters a signal to the device. The current address state immediately follows the WC state.

Current Address (CA) - As the second cycle of a 3-cycle data break, this cycle establishes the address for the transfer that takes plce in the following cycle (break state). Normally the location following the word count is read from memory into the MB, increments by 1 to establish sequential addresses for the transfers, and then transfers into the MA for the next cycle. When the word count operation is not used, the device supplies a +1 ⟶ CA Inhibit signal to the computer so that the word read during this cycle does not increment. Transfers occur at sequential addresses due to incrementing during the WC state. During this sequence the word in the MB is re-written at the same location and the MB clears at the end of the cycle. The break state immediately follows the CA state.

Break (B) - This state is entered to enact a data transfer between computer core memory and an external device, either as the only state of a 1-cycle data break or as the final state of a 3-cycle data break. When a break request signal arrives and the cycle select signal indicates a 1-cycle break, the computer enters the break state at the completion of the current instruction. Information transfers between a device-specified core memory location and the external device through the MB. When this transfer is complete, the program sequence resumes from the point of the break. The data break does not affect the contents at the AC, L, and PC.

Time States

Two major time states, designated T1 and T2, occur during each computer cycle (or major state). Major states change at the beginning of time state T2 of each cycle so that logical operations in the new major state can commence with time pulses produced during time state T1. Time pulses occur during each time state to initiate gating circuits required to perform sequential or synchronized logical operations. During each computer cycle, memory reading occurs during time state T2 and writing occurs during time state T1.

PHYSICAL DESCRIPTION

The standard PDP-8 is designed for either table-top or cabinet mounting, as specified by the customer. In the table-top configuration the computer is a single unit 34-1/16 inches high, 21-1/2 inches wide, and 21-3/4 inches deep. In the cabinet-mounted configuration the computer can be mounted in an optional DEC computer cabinet or in a standard radio rack. When mounted in a radio rack, the user must take care to prevent toppling the rack when drawing out the PDP-8 on its slides for maintenance.

The table-top PDP-8 consists of a base assembly, which houses the operator console and the power supply, and two hinged module mounting panels located above the power supply. The module mounting panels hinge at the rear and connect to the central strut of the supporting framework by a double catch. This catch operates by a locking arrangement which uses the same key as the two lock switches on the operator console. Removing the plastic cover over each module mounting panel allows access to the modules. To expose the wiring and marginal check panels, unlock the module mounting panels and swing them outward on their hinges. Three fans are mounted horizontally in the base of each hinged module mounting assembly. These fans draw air through a dust filter located beneath the power supply, pass it over the electronic components, and exhaust it through vents at the top of the plastic covers. The capacity of each fan is 105 cubic feet per minute. Signal cables from peripheral equipment, terminated in W011 connectors, enter the PDP-8 at the bottom rear of the module mounting assemblies. The W011 connectors plug into standard module receptable connectors. A 3-prong male connector mounted on the rear panel of the power supply permits a conventional line cord to connect primary power. A red indicator lamp, adjacent to the male primary power connector, lights to indicate that primary power is available. A female connector, mounted on the rear panel above the male connector, provides a convenient source of primary power for an I/O device (usually the Teletype unit). This source is switched and fused.

When the PDP-8 is to be housed in a cabinet, a number of configurations are possible, and DEC can supply suitable cabinets both for the PDP-8 and for peripheral equipment. All DEC cabinets to house the PDP-8 have french doors below the operator console for access to additional equipment. Opening the doors above the operator console and pulling the logic assembly forward on the slides provides access to the computer modules and connectors and to the back of the operator console. The module mounting panels unlock and swing outward on their hinges. A table, located just below the operator console, has legs to support the weight of the logic and operator console when they are withdrawn for maintenance. In this configuration the power supply is mounted within the cabinet and is not mounted on the slides. A typical configuration, suitable for use with an additional bay of equipment, appears in Figure 1-4. A cabinet-mount PDP-8 ordered with a DEC cabinet has simulated rosewood doors which extend from the operator console to the top of the cabinet. A rack-mount PDP-8 ordered without a cabinet, has DEC blue front panels which extend only to the top of the processor.

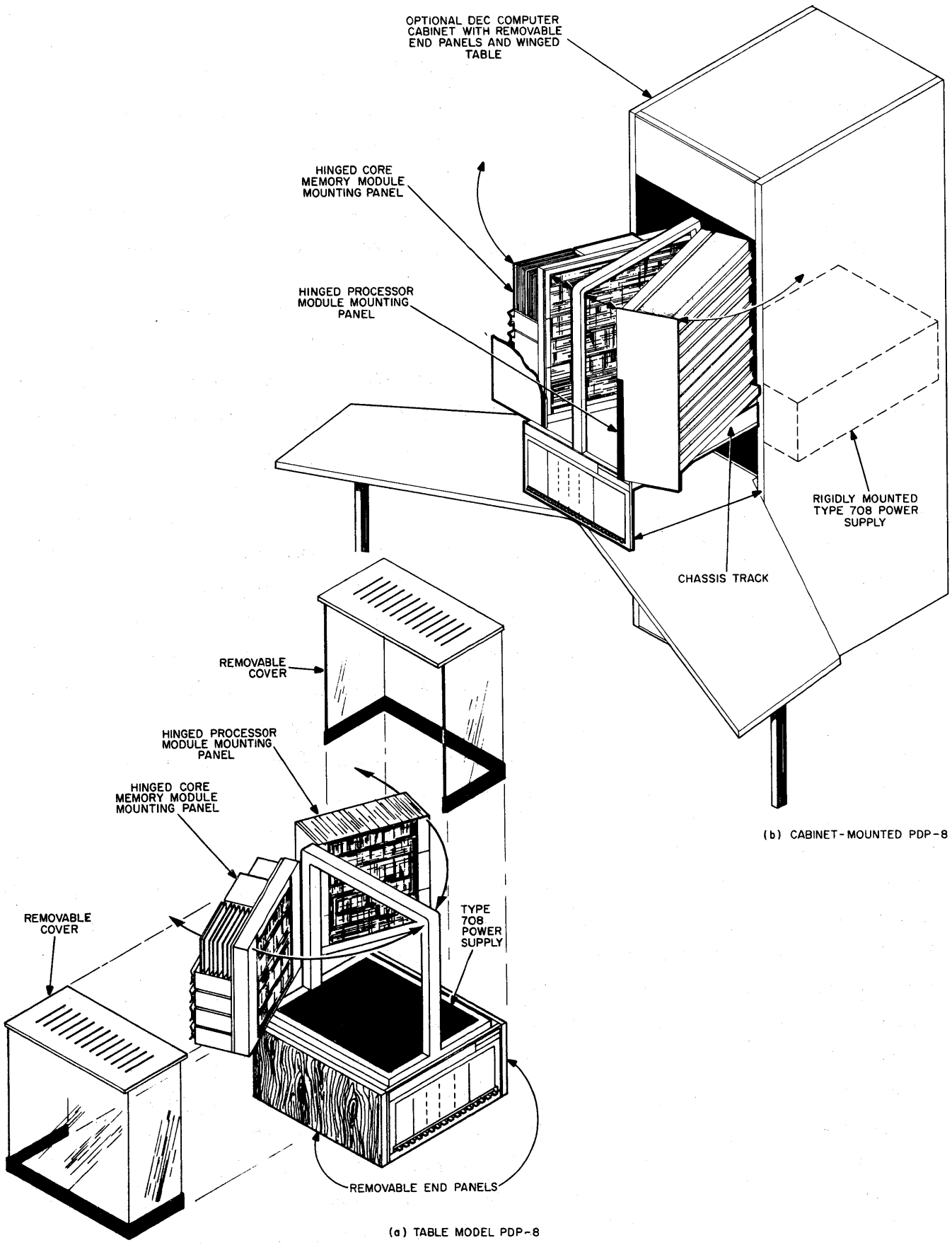


Figure 1-4 PDP-8 Mounted in a Type CAB-8B DEC Computer Cabinet

SPECIFICATIONS

Physical

Table Top PDP-8 Height	34-1/16 inches
Table Top PDP-8 Width	21-1/2 inches
Table Top PDP-8 Depth	21-3/4 inches
Table Top PDP-8 Weight	225 lbs
Cabinet Mounted PDP-8 Height	34-1/8 inches
Cabinet Mounted PDP-8 Width	19-5/8 inches (operator console)
Cabinet Mounted PDP-8 Depth	20-5/8 inches
Cabinet Mounted PDP-8 Weight	225 pounds
Teletype Height (on stand)	33 inches to top of console 44-1/4 inches to top of copy holder
Teletype Width	22-1/4 inches
Teletype Depth	18-1/2 inches
Teletype Weight (with stand)	40 lbs
PDP-8 Table (optional) Height	27 inches
PDP-8 Table Width	70-1/2 inches
PDP-8 Table Depth	44 inches
PDP-8 Table Weight	100 lbs

Electrical

Power Requirements	115v, 60 cps, single phase, 7.5 amp for standard PDP-8 (can be constructed for 220v or 50 cps upon special request)
Power Dissipation	780 watts
Digital Signal Levels	ground and −3v
Internal Circuit Potentials	+10 and −15v (logic): 30v floating (memory)

Functional

Cycle Time	1.5 μsec
Word Length	12 bits
Core Memory Size	4096 words, expandable to 32,768 in fields of 4096 words

Functional (continued)

Instructions	Eight basic instructions: six memory reference and two augmented. The augmented instructions are microprogrammed to produce more than 200 commands.
Input/Output Capability	Three command pulses can individually select and address 64 different devices.

Ambient Conditions

Operating Temperature	32 to 130°F (0 to 55°C)
Operating Humidity	0 to 90% relative humidity
Storage Temperature	32 to 130°F (0 to 55°C)
Storage Humidity	less than 90%
Heat Dissipation	2370 Btu/hr

SYMBOLS AND TERMINOLOGY

Digital Logical Symbols

Chapter 10 contains a complete list of the digital logical symbols used in illustrations and engineering drawings of this manual.

Conventions and Notations

Conventions and notations on engineering drawings and in text describing the PDP-8 are as follows:

$\vee$	Programming notation for the inclusive OR function.
$\not\vee$	Programming notation for the exclusive OR function.
$\wedge$	Programming notation for the logical AND function.
=>	Programming notation for an information transfer.
+	Design notation for the inclusive OR function and program notation for addition.
•	Design notation for the logical AND function.
⟶	Design notation for an information transfer by a single signal.

—J→	Design notation for a jam transfer of information by gating both the 1 and 0 inputs of a storage device.
A V B ⟶ A	The contents of register B OR combine with the contents of register A and store the result in register A.
A0-5 —J→ B6-11	The contents of bits 0 through 5 of register A jam-transfer into the contents of bits 6 through 11 of register B.
A2(1)	Bit 2 of register A is in the state corresponding to a binary 1, or contains a 1.
+1 ⟶ A	The contents of A increment by 1.
0 ⟶ A	Register A clears or sets to contain all binary 0's.

Other terms used in this manual are defined as follows:

set - to place a flip-flop to the state corresponding to a binary 1.

clear - to establish the state corresponding to a binary 0.

flag - a flip-flop or signal sensed by the program to indicate a specific equipment condition or status.

instruction - a computer word which causes a specific machine function and which has a distinct operation code.

microinstruction - an instruction for programming numerous machine functions by placing 1's and 0's in bits other than those which contain the operation code. Effectively, the entire word of an augmented instruction is an operation code and is decoded not only by the instruction register, but by gating circuits within the machine.

subroutine - an instruction sequence that can be called from any core memory address of the main program in order to provide a service to the main program or peripheral equipment. A subroutine usually performs recurrent operations, and thus simplifies the main program.

program interrupt - an interrupt in the main program because of a transfer of program control to a subroutine, after storing the current program count. Peripheral equipment initiates the interruption causing a subroutine to be executed. Usually the subroutine locates the equipment causing the interrupt and exchanges information with it, or services it in some way.

data break - a temporary suspension or break in the main program for exchanging data with high-speed peripheral equipment. Peripheral equipment, not the computer program, controls the information transfer.

page - a block of 128 core memory locations (200_8 addresses).

current page - the page containing the instruction being executed, as determined by bits 0 through 4 of the PC.

page address - an 8-bit number contained in bits 4 through 11 of an instruction which designates one of 256 core memory locations. Bit 4 of a page address indicates that the location is in the current page when a 1, or indicates that it is in page 0 when a 0. Bits 5 through 11 designate one of the 128 locations in the page determined by bit 4.

absolute address - a 12-bit number used to address any location in core memory.

effective address - the address of the operand. When the address of the operand is in the current page or in page 0, the effective address is a page address. Otherwise, the effective address is an absolute address stored in the current page or page 0 and obtained by indirect addressing.

command - a signal that causes a specific operation to occur as the whole or partial execution of an instruction or microinstruction.

operand - a stored number to be mathematically operated upon.

address of the operand - the location of a core memory register currently containing the operand.

PERTINENT DOCUMENTS

The following documents serve as source material and complement the information in this manual:

1. Digital FLIP CHIP Modules catalog, C-105, printed by DEC, which notes the function and specifications of the FLIP CHIP modules and module accessories for the PDP-8.

2. Programmed Data Processor-8 Users Handbook, F-85, printed by DEC, which contains computer organization information, detailed description of all instructions, basic PDP-8 programming data, and operating procedures.

3. Interface and Installation Manual, F-88, printed by DEC, which contains information for design of peripheral equipment interface and the installation of a PDP-8 system.

4. Technical Manual, Automatic Send and Receive Sets (ASR), Bulletin 273B (Volumes 1 and 2). This manual covers operation and maintenance of the Teletype unit.

5. Parts, Model 33 Page Printer Set, Bulletin 1184B, gives an illustrated parts breakdown to serve as a guide to disassembly, reassembly, and ordering parts of the Teletype unit.

6. Instruction List, F-86, printed by DEC. This is a shirt-pocket list of all memory reference instructions, all augmented instructions, the most common IOT instructions, and the ASCII code used with many I/O devices.

7. Instruction manuals and Maindec programs for appropriate input/output devices are prepared by DEC.

8. Digital Program Library Documents. Perforated program tapes and descriptive matter for the Program Assembler Language (PAL), FORTRAN, utility subroutines, and the maintenance programs (Maindec) prepared by DEC are available to PDP-8 users. The list of programs currently in the library and applicable to the PDP-8 is in Appendix 2.

One copy of the publications described in 2 through 7 and appropriate documents from the Digital Program Library are supplied by DEC with each PDP-8. Copies of the modules catalog, additional program descriptions, or additional copies of all items except 4 and 5 can be obtained from the nearest DEC district office or from:

Administrative Assistant
Field Service Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754
U.S.A.

Additional copies of items 4 and 5 can be procured from:

Teletype Corporation
5555 Touhy Avenue
Skokie, Illinois 60076
U.S.A.

ABBREVIATIONS

Listed below are the most commonly used abbreviations of registers, key operations, components, instructions, and signal names. Signal names not in this list are in Appendix 1, Signal Origins. Appendix 1 contains an alphanumerical list of all signal names which appear on drawings, together with the drawing number which contains the generating circuits for the signal.

AC	Accumulator
A/D	Analog-to-Digital (converter or convert signal)
ADD or ADDR	Address
B	Break State
BD	Bus Driver
BRK RQST	Break Request
CA	Current Address State
CLA	Clear Accumulator (Instruction or Pulse)
CLR	Clear
CM or COMP	Complement
CONT	Continue
CP	Central Processor
CS	Clock Scaler
D	Defer State
DCA	Deposit and Clear Accumulator (Instruction)
DCD	Diode-Capacitor-Diode Gate
DEP	Deposit
DF	Data Field Register
DFSR	Data Field Shift Register

DIV	Divide
DLI	Data Line Interface
DP	Deposit
E	Execute State
EAE	Extended Arithmetic Element
EX or EXAM	Examine
F	Fetch State
FLG	Flag
HLT	Halt
IF	Instruction Field
IFSR	Instruction Field Shift Register
INH	Inhibit
INST	Instruction (Key)
INT	Interrupt
INT ACK	Interrupt Acknowledge
IO	Input/Output
ION	Interrupt On
IOP	Input/Output Pulse
IOT	Input/Output (Information) Transfer
IR	Instruction Register
ISZ	Increment and Skip If Zero (Instruction)
JMP	Jump (Instruction)
JMS	Jump to Subroutine (Instruction)
L	Link
MA	Memory Address Register
MB	Memory Buffer Register
MQ	Multiplier Quotient Register
MS	Major States
MUL	Multiply
OP	Operate
OPR	Operate (Class of Instruction)
P	Parity
PA	Pulse Amplifier
PC	Program Counter
PI	Program Interrupt

PROG	Program
PWR CLR	Power Clear
SA	Sense Amplifier
SC	Step Counter (EAE)
SD	Solenoid Driver
SF	Start Field
SING	Single (Key)
SKP	Skip
SP	Special Pulse
ST	Start
STB	Strobe
SR	Switch Register
SYNC	Synchronize
TAD	Two's Complement Add (Instruction)
TT	Teletype
TTI	Teletype In (Teletype Keyboard/Reader Buffer)
TTO	Teletype Out (Teletype Teleprinter/Punch Buffer)
WC	Word Count State

REFERENCE CONVENTIONS

The DEC engineering drawing numbering system and conventions should be understood before reading beyond this chapter. Before proceeding with detailed descriptions, material in Chapter 10 and in the following sections should be studied, saving considerable reference time and preserving thought continuity through the following text.

Any reference to an engineering drawing number indicates that the drawing is in Chapter 10 of the manual. Engineering drawings are referenced by the full drawing number, unless it is assumed that the number is a block schematic. In Chapters 3 through 5 engineering drawings are referenced by the last digit only and the prefix BS-D-8-0 is assumed. For example, in these chapters BS-D-8M-0-16 is referred to simply as drawing 16. Note that the M or P following the 8 indicates that the logic is in the memory (left) or processor (right) module mounting panel.

The signal glossaries of Appendix 1 are an important adjunct to both the text and drawings. These glossaries can be used in a cross-indexing manner so that any signal and the conditions that generate it can be easily and completely referenced.

CHAPTER 2

LOGICAL FUNCTIONS

Both manual and stored-program operations of the PDP-8 are necessary to perform any complete task. The data break is the only fully automatic operation. Manual operation is normally limited to storing a Readin Mode or Binary Loader program, modifying or examining data or addresses in a prestored program, or establishing the starting conditions and initiating programmed operation of the system. Stored program operation is used in the performance of all user programs. However, for maintenance purposes and to facilitate the debugging of a new program, provision is made for manually advancing the program one cycle at a time or one instruction at a time.

The sequence in which operations occur during manual operation or during each machine cycle for stored program and automatic operation appears on the flow diagram, engineering drawing FD-D-8P-0-7.

FLOW DIAGRAM INTERPRETATION

The flow diagram illustrates the sequence of events that take place during each of the possible manual, stored program, or automatic operations. Sheet 1 of the flow diagram, containing all functions except manual operations, consists of six vertical columns. The first three columns correspond to one of the three major states in programmed operation: fetch (F), defer (D), and execute (E). The last three columns correspond to automatic operations during a data break and are represented by the word count (WC), current address (CA), and break (B) major states. Sheet 2 of the flow diagram contains the events that take place during manual operation. Horizontal rows on the flow diagram represent time states. Time proceeds from top to bottom on this diagram. The upper row represents the memory strobe during programmed and automatic operation, and represents time state SP0 during manual operation.

Events appear on the diagram as rectangular boxes joined by vertical flow lines. Operations in a sequence not specifically designated by a key name or instruction mnemonic are assumed to be common to all sequences (e.g., memory strobe in the F and D cycles, and 0 ⟶ RUN in time SP0). Branching of a common sequence into several operation chains, each associated with a specific instruction or key operation, appears as a vertical line terminated by an arrowhead on a horizontal line. Thus, in the fetch cycle, MEMORY STROBE is common to all operations, after which a branch occurs, and the next event is a JMS ⟶ IR if an INT ACK condition exists, or is MB TRANSITIONS ⟶ IR if an $\overline{\text{INT ACK}}$ condition exists. Confluence of several sequences into a further common sequence appears as several vertical lines with arrowheads that all meet a common horizontal line. A single vertical line descending from the

horizontal line to the rectangle specifies the next common event. Thus, the separate sequences associated with manual deposit and examine operations each conclude with the sequence 1 ⟶ MEM START, 1 ⟶ RUN, and 1 ⟶ RUN STOP.

Note that some events specified in the rectangles of the flow chart are conditional, others unconditional. Unconditional events appear as information transfer statements with no indication of register content. For example, key operations begin with the event 0 ⟶ RUN which occurs in time state SP0, and during a load address operation the PC clears in time state SP1. Conditional events appear as information transfer statements accompanied by one or more indications of the contents of a register. For example, during a group 1 OPR instruction, several conditional events may occur, and these appear in the leftmost sequence in time T1. The first event, +1 ⟶ PC, is unconditional. The second event, 0 ⟶ AC, occurs only if MB bit 4 contains a 1 and MB bit 6 contains a 0. When following the sequence of events in any given instruction, conditional events for which the required conditions are not met should be ignored.

To find the exact mechanism by which the processor executes an event specified in the flow diagram refer to the appropriate engineering logic diagram and the corresponding circuit description. When tracing a transfer operation, first examine the input and control gating of the register to which the transfer is being made. Thus, to trace the operation +1 ⟶ PC, first examine the logic diagram of the PC register: a command pulse designated +1 ⟶ PC strobes a set of input gates. To find how this pulse generates, examine the logic drawing of the PC control. When there is doubt where a pulse or level generates, consult Appendix 1. This appendix lists all command and control signals in alphanumerical order of designation, as well as the number of the engineering drawing on which the circuits which generate any given signal appear.

> NOTE: It is very important that maintenance personnel familiarize themselves with the flow diagram of the PDP-8. This flow diagram is the key to understanding system operation, and provides much information valuable in troubleshooting.

PREFATORY OPERATIONS

POWER and PANEL LOCK Switches

Primary power flows to the computer from the POWER and PANEL LOCK switches. With the PANEL LOCK switch in the unlocked (counterclockwise) position, turning the POWER switch to the clockwise position applies primary power to the computer. When a stored program is running, placing the PANEL LOCK

switch in the locked (clockwise) position disables the POWER switch to prevent primary power from being accidentally turned off. The PANEL LOCK switch also disables all manual keys except the SWITCH REGISTER, to prevent accidental distrubance of the program.

Power Clearing

When primary power is first applied, the capacitors of the power supply take an appreciable time to charge to the +10v and −15v levels. The processor logic circuits become operative before the supplies stabilize, but the +40v memory supplies are inhibited until the OK LEVEL relay driver in the power supply generates a negative OK level, usually when the potential on the −15v line reaches −14v. During the rise period, the $\overline{OK}$ ground level enables a 100-kc clock generating PWR CLR pulses to clear the RUN flip-flop, all the memory control flip-flops, and the Teletype control and register flip-flops. A PWR CLR pulse also generates when the START key is pressed. These PWR CLR pulses are also available at the interface to clear the registers of I/O devices. When the negative OK level appears, the 100-kc clock disables and the computer and I/O devices clear for operation.

MANUAL OPERATIONS

Keys and switches on the operator console have three functions: they permit information to be stored in core memory; they permit the contents of a specified core memory cell to be displayed for visual examination; and they permit a program to be started and stopped. Operation of the START, LOAD ADD (load address), DEP (deposit), EXAM (examine), or CONT (continue) keys causes the special pulse generator to generate four special pulse (SP) time states during which all manual operations occur. These five keys clear the RUN flip-flop during time state SP0, preventing or interrupting programmed or automatic operation. Operation of the START or CONT keys sets the RUN flip-flop to 1 during time state SP3 so that the processor begins programmed operation at the conclusion of the time state.

LOAD ADD Key

Before any program can be loaded or executed, the operator must set the starting address into the program counter (PC). Pressing the LOAD ADD (load address) key generates a KEY LOAD ADDRESS signal which starts the special pulse generator and prevents the RUN flip-flop from being set to 1 at the end of the special pulse cycle. During time state SP0, the RUN flip-flop clears. During time state SP1, the PC clears. During time state SP2, the contents of the switch register (SR) are set into the PC. If the memory extension control is in use, the contents of the INST FIELD (instruction field) switches are also set into the instruction field register (IF) and the contents of the DATA FIELD switches are set into the data field register (DF).

START Key

The START key initiates execution of a program which has been loaded into core memory. Pressing the key generates the KEY ST+EX+DP (key start OR examine OR deposit) level which starts the special pulse generator. During the cycle of the special pulse generator, the following sequence of events takes place:

1. During time state SP0, the RUN flip-flop clears, ensuring that the program does not start prematurely.

2. During time state SP1, the accumulator (AC), link (L), memory buffer register (MB), instruction register (IR), and interrupt control flip-flops clear. During this time state, the major state generator is set to fetch, and the contents of the PC jam-transfer into the memory address register (MA). At the end of this time state, the processor is ready to execute the first instruction and the PC contains the starting address.

3. During time state SP2, a MEM START pulse generates, setting the MEM ENABLE flip-flop and starting the memory timing circuits.

4. During time state SP3, the RUN flip-flop is set to 1. Programmed operation now initiated, the processor executes successive instructions until it encounters a halt command.

CONT Key

The CONT (continue) key permits a program which has temporarily halted to be restarted. Pressing this key clears the RUN flip-flop during time state SP0, generates T2B and MEM START signals during time state SP2, and sets the RUN flip-flop to 1 during time state SP3. Since operation of this key does not clear or in any way change the contents of any register, it initiates execution of the program from the conditions that currently exist.

DEP Key

Lifting the DEP (deposit) key causes the contents of the SR to deposit in memory at the address specified by the current program count. The contents of the PC then increment to permit repeated operation of the DEP key to store information at consecutive memory addresses. Note that a load address operation that sets the starting address into the PC must always precede the initial deposit operation. If the addresses at which information is to be deposited are not consecutive, a load address operation must precede each deposit operation. Pressing the DEP key initiates the following sequence of events:

1. During time SP0, the RUN flip-flop clears.

2. During time SP1, the AC, MB, and IR clear. The major state generator is set to the execute state, the contents of the PC transfer into the MA, and the contents of the PC then increment.

3. During time state SP2, the operation code for the DCA instruction (3_8) is set into the IR, the contents of the SWITCH REGISTER (SR) transfer into the AC, and a MEM START signal generates.

4. During time state SP3, the RUN flip-flop is set to 1, but is immediately reset to 0 by a T1 pulse, starting the execute cycle of the DCA instruction but ensuring that the CP halts at the end of the cycle.

5. The memory strobe is disabled so that the contents of the MB remain 0 until time state T1 of the execute cycle, when the contents of the AC transfer to the MB and the AC then clears.

6. During time state T2, the 0 state of the RUN flip-flop inhibits generation of the T2B pulse.

EXAM Key

Pressing the EXAM (examine) key causes the contents of the memory cell specified by the contents of the PC to transfer into the MB and AC for visual examination. The contents of the PC then increment so that repeated operation of the EXAM key permits examination of the contents of consecutive memory locations. Note that a load address operation must precede the first examine operation. To examine several non-consecutive memory cells, separately specify each location by a load address operation. When the EXAM key is pressed, the following sequence occurs:

1. In time states SP0 and SP1, the sequence is the same as that initiated by the DEP key.

2. In time state SP2, the operation code for TAD (1_8) is set into the IR, and a MEM START signal generates.

3. When the memory strobe pulse occurs, the contents of the specified memory cell read into the MB. During time state T1 of the execute cycle, a HALF ADD command pulse generates to transfer binary 1's from the MB into the corresponding bits of the AC.

4. During time state T2, an AC CARRY command generates which propagates carries in the AC. (Since the AC was cleared during time SP1, carries cannot occur during an examine operation.)

5. Finally, the 0 state of the RUN flip-flop inhibits generation of a T2B pulse.

STOP Key

Pressing the STOP key can halt a program at any moment. Operation of this key generates a negative RUN STOP level which clears the RUN flip-flop at the next T1 pulse. The RUN (0) level inhibits the generation of timing pulse T2B, preventing clearing of the MB and MA. Thus, the program stops just before the end of the current cycle to permit visual examination of various registers.

SING STEP and SING INST Keys

Pressing the SING STEP (single step) or SING INST (single instruction) keys steps a program one cycle or one instruction at a time, respectively. When the SING STEP key is in the up position, a negative RUN STOP level generates. Operating the CONT key sets the RUN flip-flop to 1 during time SP3 of the key cycle, and the flip-flop clears at the next T1 pulse so that processor operation halts at the end of the cycle. Thus, repeated operation of the CONT key advances the program one cycle at a time. When the SING INST key is in the up position, the RUN STOP level does not generate until an F SET level also occurs. The F SET level generates during the last cycle of the current instruction, and the processor operation halts at the end of that cycle to permit register examination.

PROGRAMMED OPERATION

The normal mode of PDP-8 operation is execution of a prestored programmed instruction sequence. A program interrupt can modify programmed operation, or a data break can temporarily suspend programmed operation. A program interrupt transfers program control from the main program to a subroutine to effect an information transfer with an I/O device or peripheral equipment. A data break is an automatic operation suspending the main program for one or three cycles to permit a high-speed I/O device to exchange information with the core memory.

Instructions

The following explanations of the functions performed during the execution of each instruction assume that the PDP-8 is energized and is operating normally under control of the main program. Each explanation begins at the start of the fetch cycle, when the address of the instruction is in the MA and a memory read operation is initiated.

Instructions performed by the PDP-8 are either memory reference instructions or augmented instructions. A memory reference instruction contains an operation code (in bits 0 through 2) and an address in core memory at which the operation is to occur (in bits 3 through 11). An augmented instruction is used when the operand is already in a register such as the AC; in this case, no memory address is required. Bits 0 through 2 of an augmented instruction contain the operation code which determines the general class of the instruction. Bits 3 through 11 of the instruction contain information which permits the required operations to occur during the two or three execution time states of a single (fetch) cycle. Operations performed in this manner are said to be "microprogrammed," since several such operations may take place during a single instruction.

Memory Reference Instructions

The format of a memory reference instruction appears in Figure 1-3(a). Instructions which reference a memory address in page 0 or in the current page occur in two cycles: fetch and execute. Instructions which reference any other page require three cycles: a fetch cycle in which the instruction word is brought out of memory and contains the effective address of the operand in the current page or page 0; a defer cycle, in which the absolute address of the operand is brought out of memory and enters the MA; and the execute cycle, in which the operand is brought out of core memory and operated on.

The following explanations of memory reference instructions assume that the instruction is directly addressed and that no break request has been initiated during its execution. (Explanations of the defer cycle and the break cycle follow the explanations of augmented instructions.)

Logical AND (AND) - The logical AND operation occurs between the contents of the addressed memory cell and the contents of the AC through a transfer of binary 0's. The result is stored in the AC and the operand is restored to memory. The original contents of the AC are lost.

First, the instruction is read into the MB from the addressed cell. Then, since no interrupt has been acknowledged, the operation code (0_8) in bits MB0 through MB2 is set into the IR. In fact, since the IR cleared at the end of the previous cycle and the operation code is 0, there is no change in the IR status. The 0 levels of the IR flip-flops decode to produce an AND level used in the control gating circuits. The following sequence of events then occurs:

1. During time state T1, the contents of the PC increment by 1.

2. The instruction rewrites into the same core memory location.

3. At the beginning of time state T2, the contents of bits MB5 through MB11 jam-transfer into the corresponding bits of the MA.

4. If bit MB4 contains a 0 and bits MA0 through MA4 are cleared, the addressed cell is in page 0 of core memory. If bit MB4 contains a 1, the addressed cell is in the current page at the location specified by the contents of bits MA0 through MA4.

5. Since bit MB3 contains a 0 (indicating direct addressing) and the instruction is not JMS, the MB clears and the major state generator is forced to the execute state.

6. The last timing pulse of the cycle, T2B, generates a MEM START pulse which initiates a new read operation. This is the end of the fetch cycle. The PC contains the address of the next instruction; the MA holds the address of the operand; the IR contains the operation code of the current instruction; the MB contains all 0's; and the major state generator is set to execute for the next cycle.

During the memory strobe portion of the execute cycle, the operand reads into the MB. No action occurs during time state T1; the instruction is restored in core memory. During time state T2, the following sequence takes place:

1. The logical AND operation occurs through a transfer of binary 0's from the MB to the corresponding bits of the AC. Bits of the AC which were in the 0 state before the transfer remain in the 0 state. Bits of the AC which were in the 1 state before the transfer remain in the 1 state only if they correspond to MB bits in the 1 state.

2. The MB clears.

3. Since there is no break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. This concludes the logical AND operation; the program is ready to fetch the next instruction from the location specified by the contents of the MA.

Two's Complement Add (TAD) - The contents of the addressed memory cell add to the contents of the AC in 2's complement arithmetic. The result of the addition is stored in the AC, and the operand (addend) is restored to memory. The original contents of the AC are lost.

During the memory strobe portion of the fetch cycle, the instruction word is read into the MB from the memory cell specified by the current contents of the MA. Then, since no program interrupt has been

acknowledged, the operation code (1_8) in bits MB0 through MB2 is set into the IR. The 1 and 0 levels of the IR flip-flops are decoded to produce a TAD gating level. Operations during the fetch cycle of a TAD instruction are identical to those during the fetch cycle of an AND instruction.

During the memory strobe portion of the execute cycle, the addend reads into the MB from the addressed memory cell. The following sequence of events then takes place:

1. During time state T1, a half-add operation occurs, in which MB bits in the 1 state cause corresponding bits of the AC to complement.

2. The operand is restored in core memory.

3. During time state T2, carries are propagated in the AC. If there is an overflow from bit AC0, the link complements. Therefore, the normal practice is to follow a TAD instruction by a test for link status.

4. The MB clears.

5. Since there is no data break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. This concludes the TAD instruction; the program is ready to fetch the next instruction from the location specified by the contents of the MA.

Increment and Skip if Zero (ISZ) - The ISZ instruction reads the contents of the addressed memory cell into the MB and then increments the contents of the MB by 1. If the incremented contents of the MB are not 0, the program proceeds to the next instruction. If the incremented contents of the MB are equal to 0, the contents of the PC increment by 1, and the program skips the next instruction.

Operations during the fetch cycle of an ISZ instruction are identical to those during the fetch cycle of an AND instruction. During the execute cycle of an ISZ instruction, the operand (2_8) is read into the MB. The E (execute) level from the major state generator combines in the MB control with the ISZ level from the IR decoder. The presence of both levels conditions a gate which triggers at time T1 to produce a pulse that causes the contents of the MB to increment by 1. In 2's complement arithmetic, a register contains 0 only when all its flip-flops are in the 0 state. Therefore, if the incremented contents of the MB are not equal to 0, bit MB0 either remains steadily in the 0 state or changes to the 1 state. In either case, there is no effect on the PC. However, if incrementing the contents of the MB changes the contents to 0, bit

MB0 changes from the 1 state to the 0 state. This transition of MB0 triggers a gate already conditioned by the E level from the major state generator and the ISZ level from the IR decoder. The gate then produces a pulse which causes the contents of the PC to increment by 1.

During time state T2 of the execute cycle, the incremented contents of the MB write back into memory and the MB clears. The contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

Deposit and Clear Accumulator (DCA) - The DCA instruction (operation code 3_8) deposits contents of the AC into the addressed memory cell and the AC clears. The original contents of the addressed cell are lost.

Operations during the fetch cycle of a DCA instruction are identical to those during the fetch cycle of an AND instruction. However, at the end of the DCA fetch cycle, when the major state generator is set to execute, the E level combines with the DCA level from the IR decoder to generate a $\overline{\text{MEM STROBE ENABLE}}$ level. This level inhibits generation of the memory strobe pulse; so although full select read current passes through the core windings of the addressed cell and switches the cores to the 0 state, the contents of the cell do not read into the MB and are therefore lost.

During time state T1 of the execute cycle, timing pulse T1 triggers a gate conditioned by the DCA level and causes the contents of the AC to transfer to the MB. Simultaneously, a second gate triggers to produce a pulse that clears the AC. During time state T2, the contents of the MB write into core memory and the MB clears. Then the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

Jump to Subroutine (JMS) - The JMS instruction (operation code 4_8) provides an exit from the main program into a subroutine. The contents of the PC (current program count) increment by 1 and write into the core memory address specified by the JMS instruction. That address transfers to the PC and increments by 1; this incremented address fetches the first subroutine instruction during the next machine cycle. When the subroutine ends, the main program reenters by a jump indirect to the address specified by the original JMS instruction. The contents of that address are now the incremented main program count, and transferring this count into the PC causes the main program sequence to continue.

The flow chart completely specifies the events which take place during execution of a JMS instruction. However, these events are easier to understand if a concrete example illustrates the flow chart. The following description of the instruction sequence assumes that the main program is in page D of core memory (current page), and that the 21st instruction is JMS page 0 cell 100. The sequence of events appears in Table 2-1 and occurs as follows:

1. During time state T2 of instruction 20 of the main program, the PC contains the address of the next instruction, cell 21 in page D (current page). This address jam-transfers into the MA.

2. When the memory strobe occurs, the contents of cell D21 read into the MB. After the memory strobe, the MB contains JMS/0/100. The JMS operation code is in bits MB0 through MB2; page 0 is specified by MB3 (0), denoting a direct address, and MB4 (0), denoting page 0. Bits MB5 through MB11 specify location 100 (of page 0).

3. During time state T1 of the JMS fetch cycle, the contents of the MB (JMS/0/100) are written back into memory in location D/21.

4. During time state T2 of the fetch cycle, the contents of bits MB5 through MB11 jam-transfer into the MA. The MA now contains D/100.

5. Because bit MB4 is 0, bits MA0 through MA4 are cleared. The MA now contains 0/100, the address specified by the JMS instruction.

6. The contents of the PC (D/21) jam-transfer into the MB, and the contents of bits MB5 through MB11 (100) jam-transfer into the PC. Although simultaneous command pulses effect this exchange, both transfers take place without any mutual interference due to the storage time of the DCD gates. The MB now contains D/21, the main program count; the PC contains D/100.

7. Because MB4 contained 0 at the time of sampling, bits 0 through 4 of the PC clear, now containing 0/100. The major state generator is set to execute.

8. Generation of the memory strobe signal is suppressed to avoid disturbing the contents of the MB.

9. During time state T1 of the execute cycle, the contents of the PC and the contents of the MB each increment by 1. The PC now contains 0/100, the address of the first subroutine instruction; the MB contains D/22, the address of the main program instruction after completion of the subroutine.

10. The contents of the MB (D/22) write into memory at location 0/100, as specified by the JMS instruction.

11. The entire contents of the PC (0/100) jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

12. When the memory strobe occurs, the first instruction of the subroutine reads into the MB from location 101 of page 0. The program then proceeds to execute the subroutine.

Jump (JMP) - The JMP instruction occurs in a single fetch cycle if the address specified by the instruction is in the current page or in page 0. If the address is in any other page, a defer cycle is also required. The address specified in the instruction word is set into the PC and then transfers to the MA, so that the next instruction is taken from this address.

During the first part of the fetch cycle, the contents of the addressed memory cell (JMP instruction) read into the MB. Then, since no program interrupt has been acknowledged, the operation code (5_8) in bits MB0 through MB2 is set into the IR. Note that during time state T1 the instruction rewrites into memory, but no other action occurs.

Operations during time state T2 depend upon whether the JMP specifies direct or indirect addressing. If indirect (MB3 is 0), the address specified in page 0 or the current page is set into the MA, the MB clears, and a defer state is established. If a direct address is specified, the contents of bits MB5 through MB11 are set into the PC. If the address is located in page 0 (MB4 is a 0), bits PC0 through PC4 are cleared. If the address is in the current page (MB4 is a 1), the contents of these bits remain unchanged. If there is no break request, the contents of bits MB5 through MB11 are also set into the corresponding bits of the MA. Bits MA0 through MA4 clear for a page 0 address, and remain unchanged for a current page address. The MB then clears. Note that the notation 0 ⟶ MB appears in the first rectangle of time state T2 on the flow diagram. This should not be interpreted to mean that the MB clears before transfer of its contents to the PC and MA. In fact, the command pulses which clear the MB and open the appropriate PC and MA input gates generate simultaneously, which is technically feasible due to storage and delay times of the gates. Finally, the IR clears, and the major state generator is set to fetch.

Augmented Instructions

There are two classes of augmented instructions: the input/output transfer (IOT), which has the operation code 6_8; and the operate instruction (OPR), which has the operation code 7_8. Augmented instructions are one-cycle (fetch) instructions which initiate various operations as a function of bit microprogramming.

TABLE 2-1 EXAMPLE OF REGISTER CONTENTS DURING A JMS INSTRUCTION

Cycle	Time	PC Contents Page 0-4	PC Contents Location 5-11	Memory Address	Memory Contents	MB Contents 0-4	MB Contents 5-11	MA Contents 0-4	MA Contents 5-11	Command
Fetch or Execute	T2	D	21	D/21	JMS/0/100			D	21	PC ⟶ MA
Fetch	T1			D/21	JMS/0/100	JMS/0	100	D	21	Memory to MB
	T2							D	100	MB5-11 ⟶ MA
								0	100	MB4(0): clear MA0-4
		D	21			D	21			PC ⟶ MB
		D	100							MB5-11 ⟶ PC
		0	100							MB4(0): clear PC0-4
										MB to Memory
Execute	T1	0	101							+1 ⟶ PC
						D	22			+1 ⟶ MB
				0/100	D/22	D	22			Memory to MB
	T2							0	101	PC ⟶ MA
				0/101	1st subroutine instruction					

Assumptions for this example:

1. Memory pages are designated 0, A, B, C, D, E...etc.
2. Each page contains locations designated 0 through 128.
3. The main program is operating in page D.
4. The subroutine is in page 0, starting at location 101.
5. All operations within one time state occur simultaneously, not sequentially.

Input/Output Transfer (IOT) - The bit assignment of the IOT instruction is shown in Figure 1-3(b). Bits 0 through 2 contain the operation code (6_8) and bits 3 through 8 form a code that enables the device selector in a given I/O device.

Three groups of IOT instructions are executed completely in a normal 1.5-μsec fetch cycle. These are the commands having a select code of 00 that apply to the program interrupt and Analog-to-Digital Converter Type 189, commands with a select code of 2X that apply to the optional Memory Extension Control Type 183, and commands having a select code of 40 that apply to the Data Line Interface Type 681. When instructions in either of these groups are executed, the instruction word reads into the MB during the memory strobe period, and the operation code is set into the IR. Detection of select codes 00 or 2X in bits MB3 through MB8 inhibits the generation of IOP pulses. Special decoding of bits 9, 10, and 11 in the program interrupt synchronization element and in the Type 183 option generates pulses that substitute for IOT commands. For example, when the select code is 00 if bit MB11 contains a 1 (ION), the INT ENABLE flip-flop sets; so the processor responds to interrupt requests from an I/O device, or if bit MB10 contains a 1 (IOF), the INT ENABLE and INT delay flip-flops clear, preventing any interruption of the program. The MB clears in time state T2. Then, if there is no break request, the contents of the PC (incremented during time state T1) are set into the MA, the IR clears, and the major state generator is set to fetch.

Any other IOT instructions use the pause facilities to extend the fetch cycle to 3.75 μsec (2.5 machine cycles) so that IOP pulses can generate, and to decode the select code by the device selector in an I/O device. When a normal IOT instruction is detected, a 1 ⟶ PAUSE signal level generates which sets the PAUSE flip-flop and stops the timing generator of the main computer cycle. The 1 ⟶ PAUSE command pulse also starts the timing chain of the IOP pulse generator which, after 0.5 μsec, permits generation of an IOP1 pulse if bit MB11 of the IOT instruction contains a 1. An IOP2 pulse generates 1 μsec later if bit MB10 contains a 1, and an IOP4 pulse generates 1 μsec after IOP2 if bit MB9 contains a 1. At a time 2.5 μsec after the generation of the 1 ⟶ PAUSE command pulse, the IOP pulse generator sets the RESTART SYNC flip-flop to 1. Changing RESTART SYNC flip-flop from the 0 to the 1 state sets the RUN flip-flop. The next clock pulse forces generation of a T2B timing pulse that sets the major state generator to fetch, and causes a MEM START pulse to occur. The MEM START pulse clears the PAUSE flip-flop, which in turn clears the RESTART SYNC flip-flop. The RUN(1) and PAUSE(0) levels enable the timing circuits and the processor resumes its normal 1.5 μsec timing cycle. These operations appear in Figure 2-1.

The IOP pulses are gated in the device selector of the addressed I/O device to produce IOT pulses that control the operation of the device, effect a transfer of information between the device and the processor, or initiate action in the processor such as clearing the AC or incrementing the PC. For details of the IOT instructions available, refer to the PDP-8 Users Handbook, F-85.

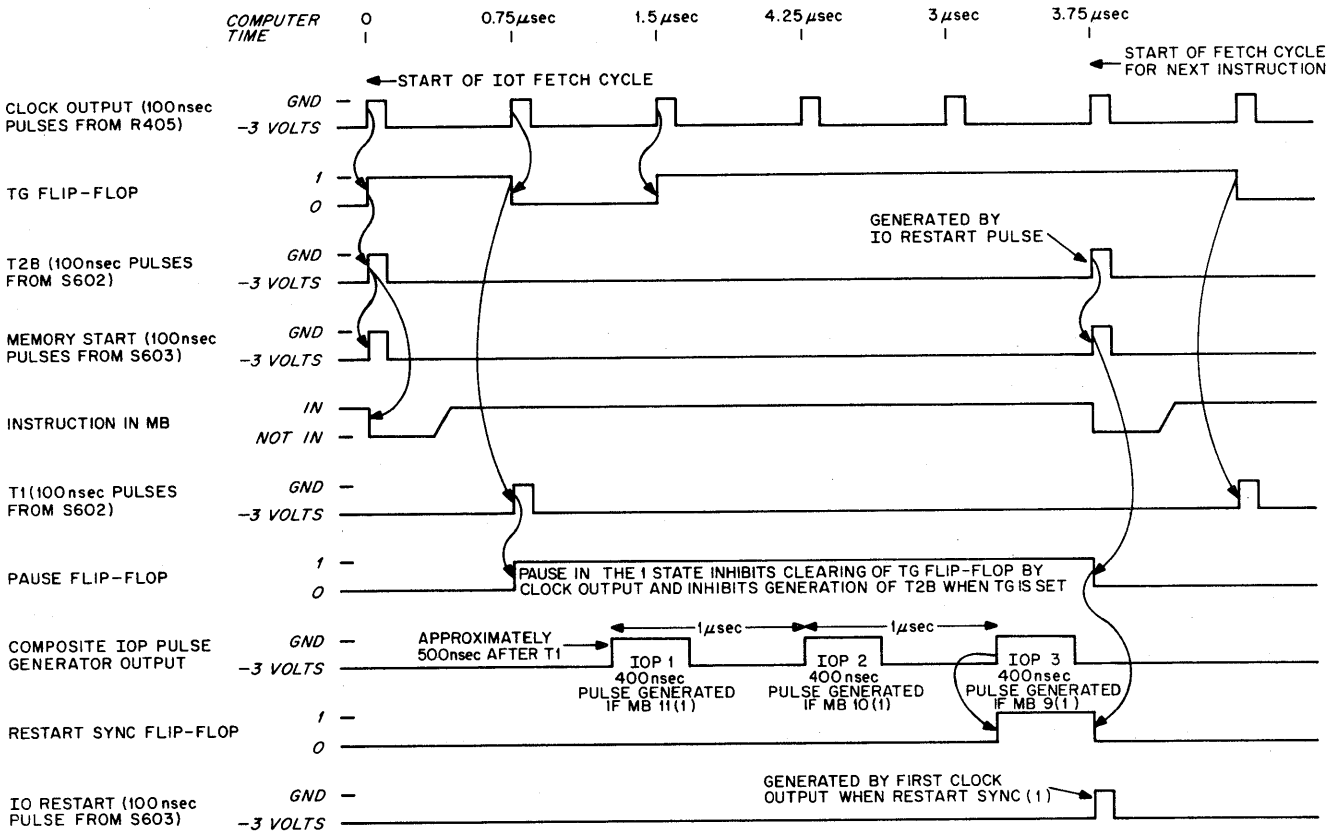


Figure 2-1 IOT Timing Diagram

Operate (OPR) - The OPR instruction consists of two groups of microinstructions. The format of both groups appears in Figure 1-3(c) and 1-3 (d). In each case, bits 0 through 2 contain the operation code 7_8. Group 1, designated by a 0 in bit 3, performs clearing, complementing, rotating, and incrementing operations. Group 2, designated by a 1 in bit 3 and a 0 in bit 11, checks the contents of the accumulator and link, and uses the result of the check to determine whether the next instruction is to be performed or skipped.

The operations specified by the group 1 OPR microinstructions may occur singly or in logical combination. It would not be logical, for example, to specify RAR and RAL simultaneously, since they are conflicting operations. The instruction word is read into the MB by the memory strobe, and the contents of the PC increment during time state T1. Thereafter, the following operations take place as a function of the contents of bits 4 through 11:

1. Clear accumulator (CLA). If bit MB4 is 1 and MB6 is 0, the accumulator clears during time state T1.

2. Clear link (CLL). If bit MB5 is 1 and bit MB7 is 0, the link flip-flop clears to 0 during time state T1.

3. Complement accumulator (CMA). If bit MB4 is 0 and bit MB6 is 1, the contents of the AC are set to the 1's complement of its original content, during time state T1.

4. Complement link (CML). If bit MB5 is 0 and bit MB7 is 1, the link flip-flop complements during time state T1.

5. Set accumulator (STA). If bits MB4 and MB6 are both 1, the AC contains all 1's during time state T1. This operation is logically equivalent to combining the CLA and CMA commands.

6. Set link (STL). If bits MB5 and MB7 are both 1, the link flip-flop is 1. This operation is logically equivalent to combining the CLL and CML commands.

Rotation and incrementation of the AC take place during time state T2 of group 1 OPR instructions. The instructions are:

1. Rotate accumulator right (RAR). If bit MB8 is 1 and bit MB10 is 0, the combined contents of the accumulator and link rotate one place right.

2. Rotate two right (RTR). If bits MB8 and MB10 are both 1, the combined contents of the accumulator and link rotate two places right.

3. Rotate accumulator left (RAL). If bit MB9 is 1 and bit MB10 is 0, the combined contents of the accumulator and link rotate one place left.

4. Rotate two left (RTL). If bits MB9 and MB10 are both 1, the combined contents of the accumulator and link rotate two places left.

5. Increment AC (IAC). If bit MB11 is a 1, the contents of the AC increment by 1. This instruction combines with the CMA microinstruction to convert a binary number in the AC to its equivalent 2's complement number.

When all the microinstructions specified by a group 1 OPR instruction are performed, the MB clears and, if there is no break request, the IR clears and the major state generator remains in the fetch state.

The operations specified by the microinstructions of group 2 OPR may be performed singly or in any logical combination. The microinstructions include clear accumulator, halt, and those which cause a skip as a function of the status of the AC and/or link. If two or more skips combine in a single group 2 OPR instruction, when bit 8 is a 0, the inclusive OR of the various skip conditions determines the skip. When bit 8 is a 1, the AND of all the inverse skip conditions determines the skip.

During the strobe portion of the fetch cycle, the instruction word reads into the MB and the operation code goes into the IR. Then, during time state T1, the contents of the PC increment by 1 if no skip is specified or if the specified conditions for a skip are not met. If a skip is specified and the required conditions are met, the contents of the PC increment by 2, causing the program to skip over one instruction. Three of the microinstructions do not cause a skip and are not affected by the contents of bit 8. These are:

1. Clear accumulator (CLA). When bit 4 contains a 1, the AC clears to all 0's.

2. OR with SWITCH REGISTER (OSR). When bit 9 contains a 1, binary 1's in the SR transfer into the corresponding bits of the AC. This transfer does not affect AC bits which already contain a 1; thus, the final contents of the AC are the inclusive OR of the 1's in both registers. Note that if the OSR and CLA microinstructions combine, the CLA operation takes place in time state T1, and the OSR operation in time state T2. Thus, the contents of the SR transfer to the AC and the original contents of the AC are lost.

3. Halt (HLT). When bit 10 contains a 1, the RUN flip-flop is set to 0 during time state T1, and the program halts at the end of time state T2. The HLT microinstruction can combine with any others in the same operate group, regardless of the event time at which they occur.

There are six conditional and one unconditional skip microinstructions. A 1 in bit 8 and 0's in bits 5, 6, and 7 specify an unconditional skip (SKP). Conditional skips fall into three pairs, in which a 0 in bit 8 specifies one microinstruction of a pair and a 1 in bit 8 the other. The pairs are:

1. Skip on non-zero link (SNL) and skip on zero link (SZL). When bit 7 is 1 and bit 8 is 0, the contents of the link are sampled, and, if the content is 1, the next instruction is skipped (SNL). When bits 7 and 8 are both 1, the skip occurs if the content of the link is 0 (SZL).

2. Skip on zero AC (SZA) and skip on non-zero AC (SNA). When bit 6 contains a 1, the contents of the AC are sampled. If bit 8 is 0, the next instruction is skipped if the contents of the AC are 0 (SZA); if bit 8 is 1, the next instruction is skipped if any bit of the AC contains a 1 (SNA).

3. Skip on minus AC (SMA) and skip on positive AC (SPA). When bit 5 contains a 1, the contents of bit AC0 are sampled. If bit 8 contains a 0, the next instruction is skipped

when bit AC0 contains a 1, indicating that the AC contains a negative 2's complement number. If bit 8 is 1, the next instruction is skipped when bit AC0 contains a 0, indicating that the AC contains a positive 2's complement number.

Indirect Addressing

In a memory reference instruction, nine bits are available for specifying the address of the operand. These are sufficient for specifying an address in the same page of memory as the instruction, or an address in page 0. Twelve bits are required to address an operand in any other page. In such a case, the address in bits 5 through 11 of the instruction word is not the absolute address of the operand, but the address of a memory location (in the current page or in page 0) in which the absolute address of the operand is stored. Further, bit 3 of the instruction word contains a 1 signifying an indirect address.

An indirectly addressed memory reference instruction requires three cycles: fetch, in which the instruction is retrieved from memory; defer, in which the absolute address of the operand is retrieved from memory; and execute, in which the operand is retrieved from memory and the specified operation is executed. The only exception to this rule is a JMP indirect which is executed in a fetch and a defer cycle.

During the fetch cycle, the instruction word reads into the MB and the operation code is set into the IR. If the instruction is AND, TAD, ISZ, or DCA, the contents of the PC increment by 1. Incrementation does not occur, however, if the instruction is an indirectly addressed JMS or JMP. During time state T2 of the fetch cycle, the current page address specified by the instruction goes into the MA. Then, since bit MB3 contains a 1, the MB clears and the major state generator is set to defer.

During the strobe portion of the defer cycle, the absolute address of the operand reads into the MB. During time state T1, if bits MA0 through MA7 are 0 and bit MB8 is 1 (indicating that the address specified by the instruction was one of the autoindexing locations 10 through 17 in page 0), the contents of the MB increment by 1 and the incremented contents rewrite into memory at the same address.

During time state T2 of the defer cycle, if the instruction is neither JMP nor JMS, the contents of the MB jam-transfer into the MA, setting the absolute address of the operand into the MA. The MB then clears, and the major state generator is set to execute.

If the instruction is JMS, the contents of the PC jam-transfer into the MB during time state T2, and the entire contents of the MB then jam-transfer back into the PC. If the instruction is JMP, during time state T2 the contents of the MB jam-transfer into the PC and the MB clears. The contents of the MB also

transfer into the MA, setting up the address of the next instruction. The IR clears, and the major state generator indicates fetch. The subsequent fetch cycle retrieves the next instruction from the location indirectly specified by the JMP instruction.

Program Interrupt

I/O devices which require several commands to accomplish an information transfer or that are too slow to have the computer wait in a skip loop for the device to complete an operation, employ the program interrupt facility. A program interrupt is similar to a JMS to address 0000. When the program enables the program interrupt, an I/O device or other peripheral equipment initiates an interrupt request, or the interrupt may initiate from a programmed IOT instruction. An interrupt can occur only on completion of the current instruction, and takes effect at the beginning of the following fetch cycle.

During the strobe portion of the fetch cycle, the operation code for JMS goes into the IR, regardless of the instruction word read into the MB. The contents of the MB then write back into the original location during time state T1. During time state T2, the MA clears and the contents of the PC jam-transfer into the MB. The major state generator then indicates execute.

During the execute cycle of the JMS, generation of the memory strobe pulse is inhibited. During time state T1, the contents of the MB (which are the current program count) write into memory at location 0. The contents of the PC then increment by 1. During time state T2, the MB clears, the contents of the PC (0001_8) jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. Thus, the next instruction will come from memory location 1. The instruction stored at this location is usually a JMP which transfers program control to the first instruction of a subroutine for identifying and servicing the interrupting device. A JMP indirect to address 0000_8 executes exit from the subroutine and reentry into the main program at the point of the interrupt.

AUTOMATIC OPERATION

Data Break

Data breaks occur as a single-cycle break state at an address specified by the requesting device, or as a three-cycle data break consisting of a word count, current address, and break state in which words in the computer core memory control the number of words transferred and the address of each transfer. The data break allows a high-speed I/O device to transfer data with core memory without disturbing the program or active registers. The device requesting a data break supplies a BREAK REQUEST, CYCLE SELECT, TRANSFER DIRECTION, a 12-bit data (core memory) address, and a 12-bit data word (when the transfer

direction is into the computer). When a break request occurs, the address designated by the device jam-transfers into the MA during time T2 of the last cycle of the current instruction, and the major state generator is set to the WC state if the CYCLE SELECT signal is at ground, or is set to the B state if this signal is at −3v. The program delays for the duration of the data break, commencing in the following cycle. Note, however, that a break request is granted only after completion of the current instruction. A break occurs only under the following conditions:

1. At the end of the fetch cycle of an OPR or IOT instruction, or of a directly addressed JMP instruction.

2. At the end of the defer cycle of an indirectly addressed JMP instruction.

3. At the end of the execute cycle of a JMS, DCA, ISZ, TAD, or AND instruction.

Single-Cycle Data Break

One-cycle breaks transfer a data word into the computer core memory from the device, transfer a data word into a device from the core memory, or increment the contents of a device-specified memory location. The timing of operations in these three types of break appears in Figures 2-2, 2-3, and 2-4.

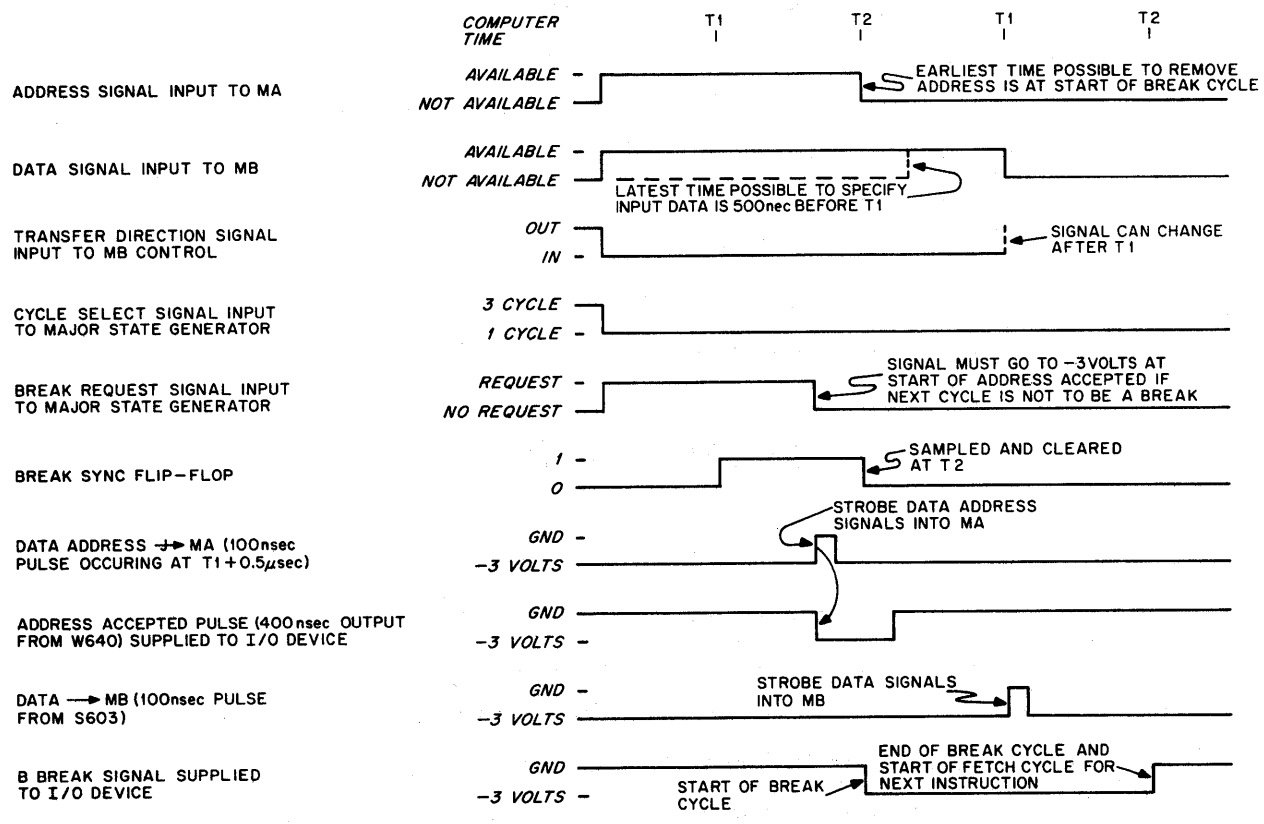


Figure 2-2 Single-Cycle Data Break Input Transfer Timing

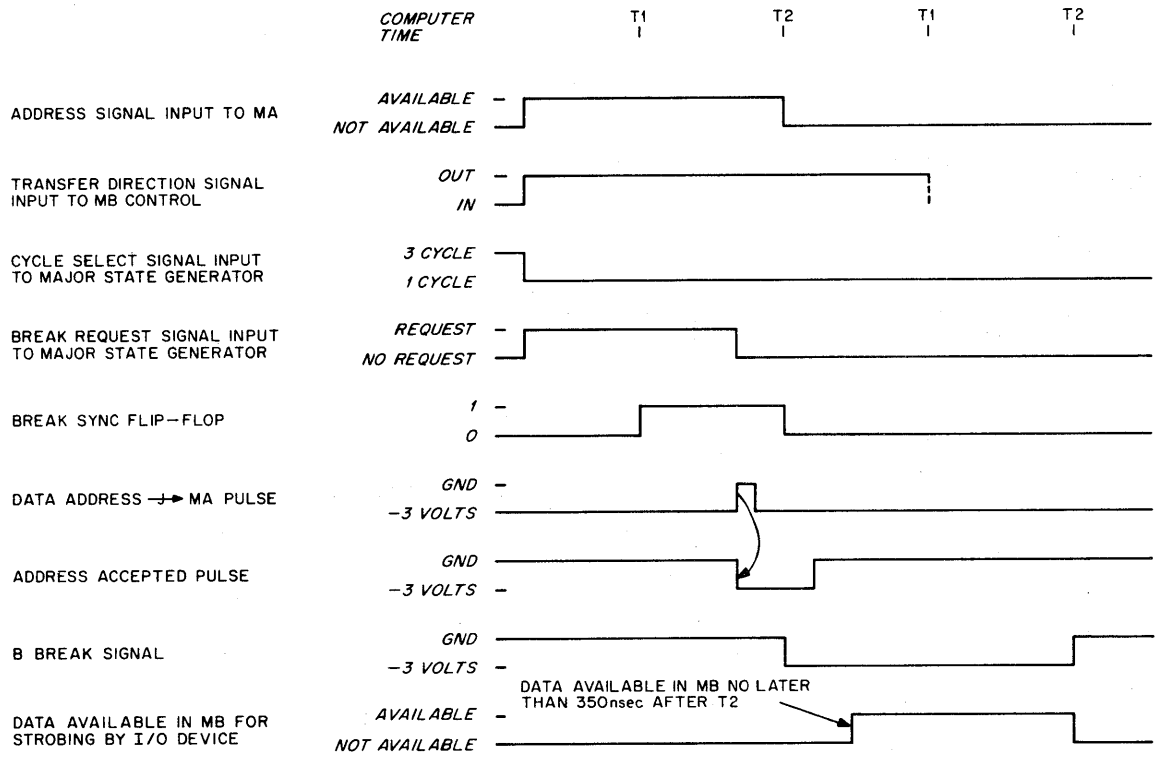


Figure 2-3 Single-Cycle Data Break Output Transfer Timing

In each of these types of data break one computer cycle is stolen from the program for each transfer; break cycles occur singly (interleaved with the program steps) or continuously (as in a block transfer), depending upon the timing of the BREAK REQUEST signal.

During the strobe portion of the break cycle, the contents of the addressed cell read into the MB if the transfer is out of the computer (into the I/O device). However, if the transfer is into the computer, generation of the memory strobe pulse is inhibited so that the MB (cleared during the previous cycle) remains cleared. During time state T1 of the break cycle, information transfers from the output data register of the I/O device into the MB and writes into memory. In the case of an outward transfer, the write operation restores the original contents of the addressed cell to memory.

During time state T2 of the break cycle, the MB clears. If there is a further break request, another break cycle may initiate. If there is no break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. The program is then ready to execute the next instruction.

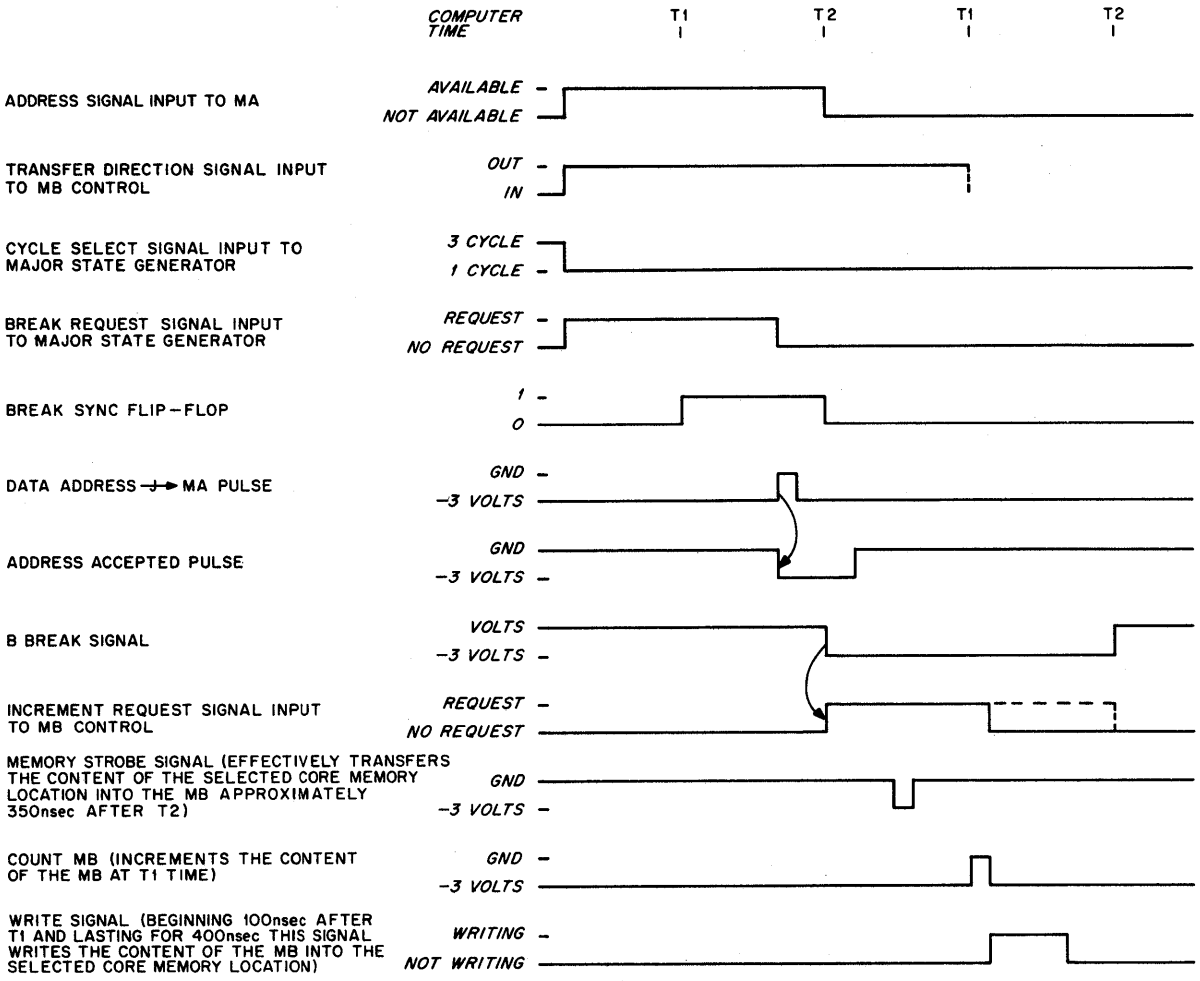


Figure 2-4 Single-Cycle Data Break Memory Increment Timing

Three-Cycle Data Break

The three-cycle data break facility provides an economical method of controlling the transfer of data between the computer core memory and fast peripheral devices. Transfer rates in excess of 220 kc are possible using this feature of the PDP-8.

The three-cycle data break differs from the one-cycle break in that a ground-level CYCLE SELECT signal is supplied and the WC (word count) state is entered to increment the fixed core memory location containing the word count. The device requesting the break supplies this address as in the one-cycle break, except that this is a fixed address supplied by wired ground and -3v signals rather than from a register. The only restriction on this address is that it must be an even number (bit 11 = 0). Following the WC state a CA (current address) state occurs in which the location following the WC address (bit 11 = 1 after + 1⇒ PC) is read, incremented by one, restored to memory and used as the transfer address (by MB ⇒ MA). Then the normal B (break) state is entered to effect the transfer. Figure 2-5 indicates the timing of these operations.

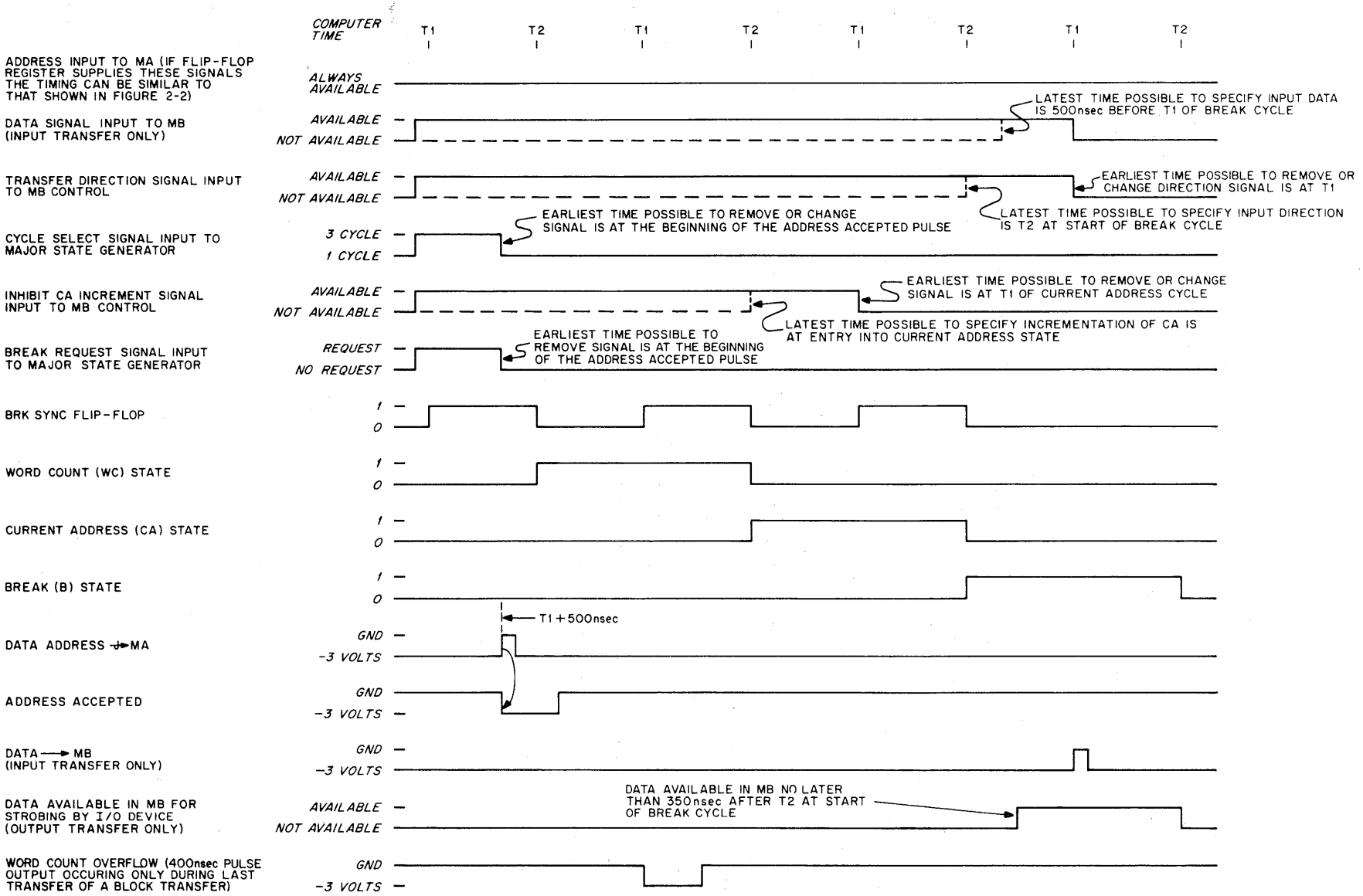


Figure 2-5 Three-Cycle Data Break Timing

Word Count State - When this state is entered the core memory address specified by the external device reads into the MB during time state T1. The word in the MB increments by 1 to advance the word count and if the word becomes 0 when incremented, a WC OVERFLOW pulse generates and flows to the device. During time T2 the incremented word rewrites in memory, the MB clears, the contents of the MA increment by 1 to establish the next location as the address for the following cycle, and the major state generator is set to the current address state.

Current Address State - Operations during the second cycle of the three-cycle data break depend upon the condition of the INCREMENT CA INHIBIT (+1 ⟶ CA INHIBIT) signal supplied to the computer from the external device. During T1 the address following the word count reads into the MB. If the INCREMENT CA INHIBIT signal is at ground potential, no further operations occur during T1. If this signal is at −3v, the contents of the MB increment by 1 during T1 to advance the address of the transfer to the next sequential location. During T2, the contents of the MB rewrite into core memory, the address word in the MB jam-transfers into the MA to designate the address to be used in the succeeding cycle, the MB clears, and the major state generator is set to the break state.

Break State - The actual transfer of data between the external device and the core memory, through the MB, occurs during the break state, as during a single-cycle data break, except that the current contents of the MA, not the device itself, determine the address.

CHAPTER 3

PROCESSOR

Logic circuit elements of the processor perform the major arithmetic, logic, and control functions of the PDP-8. The processor performs all operations of the PDP-8 except those directly concerned with data storage and retrieval in core memory and information exchanges with I/O equipment. In performing these operations, the processor draws instructions from core memory and executes them by sequentially establishing one or more major control states. Each control state lasts the duration of one computer cycle, in which there are two time states.

Functional operation of the processor is similar to a 3-dimensional matrix. As in the matrix, X, Y, and Z coordinates must be specified to locate a given point, so within the processor an instruction, a major state, and a timing pulse determine the specific logic function performed. A change in any one of these determinants changes the resultant logical operation. In general, the current instruction and current state determine the major state, except that a data break request originating in peripheral equipment initiates the word count or break state. The word count or break state occurs only after the current instruction is completed. Execution of each of the six basic memory reference instructions requires two or three of the major states. Execution of an augmented instruction requires only one state, although an IOT instruction increases the normal timing cycle. The sequence of operations during execution of each of the eight basic instructions is described in detail in Chapter 2 of this manual.

> NOTES: Throughout Chapters 3, 4, 5, and 6 all drawing references in headings and in text are to the block schematic engineering drawings of the computer, unless otherwise stated. Block schematic diagrams carry the identifying code BS-D-8-0-X, where X is the number of the specific drawing. For brevity, only the drawing number (X) is given as a reference to these drawings. Drawings carrying any other identification code are referenced by the complete identification number.
>
> Several of the module types in the PDP-8 belong to an S series which is not described in the Digital FLIP CHIP Modules Catalog, C-105. Series S modules are logically identical to R series modules described in the catalog. Except for a faster transistor and a lower value of load resistor in the output stage, S series modules are identical to R series modules.

POWER CLEAR GENERATOR (9, 16)

During the power turnon sequence, the power clear generator produces repeated PWR CLR (power clear) pulses at a repetition rate of 100 kc. Pressing the start key also produces a single PWR CLR pulse. These

pulses clear the PAUSE flip-flop (10), all the memory control flip-flops, all the Teletype control flip-flops, and the TTI and TTO registers of the Teletype control. The PWR CLR pulses buffered by a pulse amplifier arrive at the interface connectors as the negative B POWER CLEAR pulses for clearing registers and control flip-flops of peripheral equipment.

During the power turnon sequence, potentials on the +10v and −15v supply lines rise relatively slowly because of the large amount of filter capacitance employed (210,000 μf in the −15v supply). Until the potential on the −15v line reaches −14v, the memory read/write and inhibit power supplies are disabled, and the PWR STATUS signal from the Type 708 Power Supply is at ground level. However, the memory and processor logic circuits become operative when the potential on the −15v line reaches approximately −8v. The PWR STATUS ground level inverts to produce a negative $\overline{\text{PWR OK}}$ level at inverter output terminal PB30F (9). The $\overline{\text{PWR OK}}$ level has two functions:

1. It inverts again to produce a RUN STOP ground level at inverter output terminal PD31F. The RUN STOP level in turn inverts to produce a negative RUN STOP level at inverter output terminal PB33D. During the power turnon sequence, the RUN STOP level clears the RUN flip-flop at every computer clock pulse to ensure that transients within the machine do not prematurely start programmed operation.

2. It enables the Type R401 Variable Clock at location PD30. The 100-kc pulses at terminal PD30D gate with the RUN (0) level to produce the positive PWR CLR pulses.

When the rising potential on the −15v supply line reaches −14v, the memory current supplies become enabled and the PWR STATUS signal changes to −3v. This action disables the variable clock and removes the RUN STOP level. Generation of the PWR CLR pulses ceases and the processor is ready for manual or programmed operation. The START key also generates one PWR CLR pulse.

SPECIAL PULSE GENERATOR (9)

The special pulse generator, shown in the upper portion of engineering drawing 9, provides the timing pulses required to initiate functions during manual operations. There are four sequential special pulses, designated SP0 through SP3.

Any key except the STOP key starts the special pulse generator. The key produces ground level which inverts in module PB31 and causes the Schmitt trigger in module PA36 to change state. The negative-going transition which appears at the output of module PA36 inverts to produce timing pulse SP0.

The SP0 triggers a one-shot in the Type R302 Delay module in PA35. Throughout the 4-μsec period during which the one-shot is in its unstable state, a negative SP STOP level is present at terminal PA35M. This level, one input to a transistor NOR gate, produces a ground RUN STOP level, which in turn produces a negative RUN STOP level at terminal PB33D. During programmed operation of the processor the RUN STOP level clears the RUN flip-flop at the next clock pulse if the PAUSE flip-flop is set to 1 and the RESTART SYNC flip-flop clears, or at the next occurrence of time state T1 if the PAUSE flip-flop clears to 0. (For further details, refer to the description of the Run and Pause Control.) If the program is not running when the key is operated, the SP STOP level has no effect.

At the conclusion of the 4-μsec delay period, the one-shot reverts to its stable state, and the positive-going level transition at terminal PA35M triggers pulse amplifier RSTU in the Type S603 module at location PA33. The positive SP1 timing pulse which appears at terminal PA33T inverts to produce a negative SP1 timing pulse. Both the positive and the negative SP1 timing pulses clear registers and effect information transfers. (Refer to flow diagram FD-D-8P-0-7 for a listing of these operations, and to the description of register controls in this chapter for operational details.)

The transition which produces the SP1 pulses also triggers a second one-shot in the Type R302 module at location PA35. At the conclusion of the 1-μsec delay period of this one-shot, a positive-going level transition appears at terminal PA35V. This transition functions as timing pulse SP2, which performs further information transfers and, during certain key operations, initiates a memory cycle to deposit or retrieve information.

The SP2 pulse triggers one-shot EM in the Type R302 module at location PA34. At the conclusion of the 1-μsec delay period, a positive-going level transition occurs at terminal PA34M. This transition functions as timing pulse SP3 and, in all key operations except a load address operation, sets the RUN flip-flop to 1 to start the computer.

TIMING SIGNAL GENERATOR (9)

The timing signal generator provides all timing pulses required to perform logical operations during programmed operation of the computer. The timing signal generator appears on the right side of engineering drawing 9 and consists of a crystal clock, the TG (timing generator) flip-flop, pulse amplifiers, and gates. The computer cycle lasts 1.5 μsec, and divides into two time states designated T1 and T2. At the beginning of time state T1 in every cycle, an ungated pulse designated T1 generates. During execute cycles only, a gated pulse designated T1E generates concurrently with the T1 pulse. At the beginning of time state T2, the ungated timing pulse T2A always generates. The gated pulses T2B and T2E may also generate concurrently. Pulse T2E occurs only during an execute cycle. Pulse T2B occurs during every cycle of

programmed operation except cycles immediately preceding a halt or a pause. Before a halt or a pause, generation of pulse T2B is inhibited, retaining information set into registers during the current cycle for sampling or visual examination.

Clock and TG Flip-Flop

The Type R405 Crystal Clock module at location PB35 produces standard positive 100-nsec pulses at a repetition rate of 1,333,333 pps. Each positive pulse complements the TG flip-flop, provided that the RUN flip-flop is set to 1 and the PAUSE flip-flop is set to 0.

A ground level permanently conditions the DCD set gate of the TG flip-flop. The reset DCD gate, however, is conditioned by a ground level only when negative RUN (1) and PAUSE (0) levels are both present at the inputs of NAND gate RSU in module PB32. If either of these levels is at ground, the reset gate of the TG flip-flop is inhibited, and the flip-flop remains in the 1 state. The crystal clock runs continuously while power flows to the processor logic circuits.

T1 Pulses

When the TG flip-flop is reset to 0, the positive-going transition at terminal PB34J triggers pulse amplifier circuit DEFH of the Type S603 module at location PB36. A positive T1 pulse appears at terminal PB36F and is distributed to the logic circuits of the processor. A negative T1 pulse, required in certain circuits, appears at inverter output terminal PB33L.

A ground E (execute) level from the major state generator conditions the DCD input gate of pulse amplifier circuit DEFH in module PB33. This ground level is present only during an execute cycle; during any other major state, a negative $\overline{E}$ level inhibits the gate. During the execute cycle, the transition of the TG flip-flop from the 1 to the 0 state triggers the DCD gate, and the pulse amplifier produces a positive T1E pulse at terminal PA33F. A negative T1E pulse appears at inverter output terminal PB33N.

T2 Pulses

When the TG flip-flop is set to 1, a positive-going level transition of the 1 output at terminal H of the flip-flop goes to three DCD gates. A ground permanently conditions gate KL in module PB36, and this gate triggers each time the TG (1) transition occurs. The associated pulse amplifier circuit produces the positive timing pulse T2A at terminal PB36M.

A ground E level from the major state generator conditions gate KL in module PA33. During an execute cycle, the TG (1) transition triggers this gate, and the associated pulse amplifier circuit produces positive timing pulse T2E at terminal PA33M.

A ground RUN (1)·PAUSE (0) level from terminal PB32U conditions gate PR of module PC30. When the processor is executing a program and the IOP generator is not in operation, this gate is conditioned. In each cycle the associated pulse amplifier produces positive timing pulse T2B at terminal PC30U. A programmed halt instruction clears the RUN flip-flop during time state T1, inhibiting gate PC30PR and suppressing pulse T2B. An IOT instruction sets the PAUSE flip-flop to 1, suppressing timing pulse T2B and maintaining the TG flip-flop in the 1 state. The program therefore pauses before time state T2 ends. At the end of the pause, an IO RESTART pulse arrives at terminal PC30V to trigger the pulse amplifier and produce pulse T2B, after which the program resumes. Timing pulse T2B also generates when the operator presses the CONT key. In this case, the KEY CONT level conditions DCD gate ST, triggered by special timing pulse SP2. The resulting T2B pulse initiates a MEM START pulse.

MEM START Pulse

The MEM START pulse initiates memory operation. Timing pulse T2B arrives at the diode input of pulse amplifier VTU in the Type S603 module at location PB36. The MEM START positive pulse appears at terminal PB36T and goes to the memory control circuits in the core memory system, where it initiates a read operation. The MEM START pulse also generates during a manual start, examine, or deposit operation. When the operator presses the START, EXAM, or DEP key, the KEY ST+EX+DP ground level conditions the DCD input gate of the mem start generator. Special timing pulse SP2 triggers the gate, and the associated pulse amplifier produces the MEM START pulse at terminal PB36T.

IOP GENERATOR (10, 16)

The IOP generator consists of a gated timing chain of delay modules initiated during an IOT instruction. When initiated, the timing chain produces a sequence of IOP pulses as determined by the contents of bits 9, 10, and 11 of the instruction. This circuit element consists of two Type R302 Delay modules at locations PA34 and PC34 and one Type S603 Pulse Amplifier module at location PC33. Each delay module contains two delay one-shots; the pulse amplifier module contains three pulse amplifiers.

Timing of the IOP pulses allows I/O equipment to perform sequential operations, initiated by each pulse within one instruction. The IOP pulses are spaced 1 μsec apart; thus, IOT instructions take longer than the normal 1.5-μsec cycle time. Therefore, when the IOP generator is initiated, the run and pause control delays the cycle for three clock pulses (2.25 μsec). (1.5-μsec normal cycle time +2.25-μsec delay = 3.75-μsec IOT cycle time.)

The 1 ⟶ PAUSE pulse initiates operation of the timing chain. A 6-input negative NAND diode gate produces this pulse at terminal PC35J. The gate triggers to produce the pulse when the T1 pulse occurs if all of the following conditions exist:

1. The IOT signal is at −3v, indicating that the current instruction is an IOT.

2. The F(1) signal is negative, indicating that the major state generator is in the fetch state.

3. The $\overline{\text{PROCESSOR IOT}}$ signal is negative, meaning the instruction does not have the select code of 00 used with the program interrupt control and the 189 Analog-to-Digital Converter.

4. The $\overline{\text{MEM EXT}}$ signal is negative, meaning that the instruction is not a 1.5-μsec IOT used with the 183 Memory Extension Control.

5. The $\overline{\text{TT INST}}$ signal is negative, meaning that the instruction is not a 1.5-μsec IOT used with the 681 Data Line Interface.

These conditions simply enable generation of the 1 ⟶ PAUSE pulse, and subsequent entry into a 3.75 μsec cycle for all IOT instructions except those which use the normal 1.5-μsec machine cycle or a special timing cycle determined by the device execution time.

One-shot NV is set to give a delay of 0.5 μsec; at the end of this time, the one-shot reverts to its stable state and the positive-going level transition appearing at terminal PA34V triggers one-shot EM in the same module. If bit MB11 contains a 1, the transition also triggers the DCD input gate of pulse amplifier circuit DFH in module PC33. The pulse amplifier produces an IOP 1 pulse at terminal PC33F; this pulse goes to pulse amplifier circuit DHJ of module MC31 in the memory assembly. A negative IOP 1 pulse appears at interface connector terminal MF34K (16, C7), where it is available to the device selectors of I/O equipment.

One-shot EM of module PC34 gives a delay of 1 μsec. At the end of this time, the one-shot reverts to its stable state and the positive-going level transition appearing at terminal PC34M triggers one-shot NV in module PC34. If bit MB10 contains a 1, the transition also triggers pulse amplifier KMN in module PC33, and a positive IOP 2 pulse appears at terminal PC33M. This pulse operates pulse amplifier KNP in module MC31, causing a negative IOP 2 pulse to be applied to interface connector MF34M.

One-shot NV of module PC34 gives a delay of 1 μsec. At the end of this time, the one-shot reverts to its stable state and sets the RESTART SYNC flip-flop to 1, if no RUN STOP signal has been generated in the meantime. At the same time, if bit MB11 contains a 1, the transition triggers pulse amplifier RSTU in module PC33 to produce an IOP 4 pulse at terminal PC33T. Pulse amplifier RUV in module MC31 produces a negative IOP 4 pulse which appears at interface connector terminal MF34P.

RUN AND PAUSE CONTROL (9, 10, 16)

The run and pause control starts, stops, and temporarily interrupts programmed operation of the computer. The RUN flip-flop, when set to 1, enables operation of the timing signal generator, and when cleared to 0, disables the timing signal generator. The PAUSE flip-flop is set to 1 by most IOT instructions. When set to 1, the PAUSE flip-flop prevents advance of the program for a period of 2.5 μsec, during which one or more IOP pulses initiate to control the operation of peripheral equipment. At the conclusion of the pause, IO RESTART, T2B, and MEM START pulses restart operation of the computer and clear the PAUSE flip-flop.

Run Control (9)

The RUN flip-flop provides a negative RUN (1) level which, in combination with a negative PAUSE (0) level, enables the TG flip-flop to be complemented at every clock pulse, thereby generating timing pulses. If either of these levels is at ground, the reset gate of the TG flip-flop is inhibited, and the computer stops in time state T2. The RUN flip-flop is set to 1 by the reset gate to perform functions initiated by operating the START, DEP, EXAM, or CONT keys, or is set when the RESTART SYNC flip-flop changes from the 0 to the 1 state.

Special timing pulse SP3 sets the RUN flip-flop when a ground $\overline{\text{KEY LOAD ADDRESS}}$ level conditions the set DCD gate. The $\overline{\text{KEY LOAD ADDRESS}}$ level is present except when the LOAD ADD key is pressed; inverter output terminal PB33J (9, B1) is then driven to −3v and inhibits the RUN set gate. The RUN flip-flop is also set by the leading edge of the RESTART SYNC (1) level which arrives at the direct-set input of the flip-flop.

A positive pulse at output terminal S clears the RUN flip-flop when a HLT command is executed or when required by functions controlled by manual key operations. This flip-flop also clears through the reset gate for execution of an IOT instruction using the pause feature.

The RUN flip-flop clears during a pause condition if a RUN STOP level generates between the time the PAUSE flip-flop is set to 1 and the time the RESTART SYNC flip-flop is set. The RUN STOP, PAUSE (1), and RESTART SYNC (0) negative levels NAND combine to condition the DCD reset gate of the RUN flip-flop. The gate triggers at the next clock pulse and clears the RUN flip-flop. Under all other conditions of manual or stored program operation, the RUN flip-flop clears if a RUN STOP level conditions NAND gate KLN in module PA27. The gate, triggered by the next T1 timing pulse, clears the flip-flop. A 6-input NOR gate generates a RUN STOP level if any one of the following conditions exist:

1. During the power turnon sequence, a ground POWER STATUS level inverts in module PB30 to produce a negative $\overline{\text{PWR OK}}$ level. This level again inverts in module PD31, and inverter output terminal PD31F goes to ground, producing the ground RUN STOP level. The RUN STOP level generated during power turnon is not produced after the −15v supply line rises to −14v and the memory read/write and inhibit supplies rise to within 3v of their proper values.

2. During a manual examine or deposit operation, a KEY ST+EX+DP level produces the ground RUN STOP level.

3. When the SP STOP level is produced by the special pulse generator.

4. Whenever the SING STEP switch is activated (in the up position).

5. When the SING INST switch is activated (in the up position), the inverted SINGLE INST level NAND combines with the F SET level from the major state generator to produce a RUN STOP level at the end of each instruction.

6. During execution of a programmed HLT command. The halt microinstruction is included in a Group 2 OPR instruction by inserting a 1 in bit 10 of the instruction. The MB10 (1) level NAND combines with an OP2 pulse generated in control to produce the RUN STOP level.

Pause Control (10)

The pause control, operated by the IOP generator, prevents advance of the timing signal generator, extending the cycle time of an IOT instruction by 2.25 μsec. The pause control consists of a PAUSE flip-flop, a RESTART SYNC flip-flop, and associated gating circuits. The negative PAUSE (0) level (with the RUN (1) level) enables the timing generator when the flip-flop is set to 1, the ground level PAUSE (0) stops the program in time state T2. A negative PAUSE (1) level also drives the PAUSE indicator on the operator console.

The PAUSE flip-flop initially clears at power turnon by positive PWR CLR pulses arriving at diode OR gate input PD34R (10, A8), or during a key operation by special timing pulse SP1 applied to terminal PD34P. After a pause operation, a MEM START pulse at the direct clear input at terminal PC32K resets the flip-flop at T2 time.

A 1 ⟶ PAUSE pulse applied to the DCD gate pulse input at terminal PC32N sets the PAUSE flip-flop.
The 1 ⟶ PAUSE pulse generates in the IOP generator as described previously in this chapter.

The 1 ⟶ PAUSE command pulse also starts the IOP generator, and after 2.5 μsec the generator produces a pulse which sets the RESTART SYNC flip-flop if no RUN STOP level generates in the meantime. The RESTART SYNC (1) level conditions the DCD input gate of pulse amplifier circuit RTU of the Type S603 module in location PA29. The next clock pulse triggers the DCD gate and the pulse amplifier produces an IO RESTART pulse at terminal PA29T. This pulse causes the timing generator to produce timing pulse T2B. The reappearance of the PAUSE (0) level restores the timing generator to normal operation, and the program continues.

INSTRUCTION REGISTER (6)

The instruction register is a 3-bit register consisting of a Type S203 Triple Flip-Flop module in location PB28. A Type S151 Binary-to-Octal Decoder module in location PB27 decodes the bit combination stored in this register. A ground applied to terminal PB27D permanently enables the decoder. Each output signal from the decoder flows to an inverter in module PA21 or PB26 to produce a ground level and a negative level for each of the following signals and their complements: AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR. These signals correspond to octal numbers 0 through 7, respectively, stored in binary form in the instruction register. The instruction signals and their complements gate the control logic throughout the processor.

Pulse amplifier circuit PVSUN in the Type S602 module in location PB20 clears the instruction register flip-flops collectively. During manual start, examine, or deposit operations, a KEY ST+EX+DP ground level applied to terminal PB20R conditions a DCD input gate which special timing pulse SP1 triggers clearing the instruction register in preparation for programmed operation or to be jam set with TAD or DCA instructions. During execution of a program the F SET level from the major state generator conditions a second DCD gate of this pulse amplifier which is triggered by timing pulse T2B. Thus, the instruction register clears upon completion of the current instruction. During a data break the leading edge of the B(1) level triggers the pulse amplifier to clear the IR. The B(1) level is the direct output of the major state generator, so the positive-going excursion of this level occurs at T2 time when the break state is entered.

The instruction register flip-flops are set individually, as follows:

1. During the fetch cycle of any instruction, flip-flops IR0 through IR2 are set to the operation code contained in bits MB0 through MB2. The F(1) level from the major state generator conditions a NAND gate associated with each IR flip-flop. Gates enabled by a 1 output signal from the corresponding MB flip-flop produce a ground level at their output terminals and force the associated IR flip-flop to the 1 state by pull-over action.

Note, however, a $\overline{\text{INT ACK}}$ (indicating that a program interrupt will not occur during the cycle) level as well as the F(1) and MB(1) levels must condition the gates associated with flip-flops IR1 and IR2.

2. At the beginning of a program interrupt, the INT ACK (interrupt acknowledged) level combines with the F(1) level to set flip-flop IR0 only. The $\overline{\text{INT ACK}}$ level, at ground potential, disables the input gates of flip-flops IR1 and IR2. Thus, when an interrupt is acknowledged, the processor sets the operation code 4_8 into the IR, regardless of the code in bits MB0 through MB2. This action forces execution of a JMS instruction.

3. Flip-flop IR1 is set during a manual deposit operation. The DCD input gate of the flip-flop, conditioned by a KEY DP level from the DEP key, is triggered by special timing pulse SP2. At the same time, flip-flop IR2 is set. This operation sets the DCA operation code into the IR.

4. Flip-flop IR2 is set during a manual deposit or examine operation. A KEY EX+DP level from the key circuits conditions the flip-flop DCD input gate which is triggered by special timing pulse SP2. During a deposit operation, flip-flop IR1 is also set, forcing a DCA instruction into the IR. During an examine operation, when only flip-flop IR2 is set, a TAD instruction is forced into the IR.

MAJOR STATE GENERATOR (6, 10)

The major state generator consists of two Type S284 Quadraflop modules at locations PB25 and PC02, and associated input gating. Pulsing an appropriate input terminal can set a quadraflop to any one of four stable states. Connections from the active terminal (H) of one module to the disable terminal (V) of the other module ensure that only one state is set at a time. The standard PDP-8 uses only six of the eight available states. These states, and complementary output signals are designated fetch (F), defer (D), execute (E), word count (WC), current address (CA), and break (B). Adding the 681 Data Line Interface option to the system activates the two remaining states, designated status (S) and character (C). Refer to the description of the 681 in this chapter for an explanation of these states.

A major state is established for each computer cycle; states change for each cycle as required to execute instructions. States are set at T2 time of each cycle and entry into each state is determined by the instruction being performed, the current state, and the condition of the data break request signal received

from an external device. Only the fetch and the break cycles can repeat in consecutive machine cycles. Manually initiated operations utilize the F state; programmed operations use the F, D, and E states; and automatic data break operations use the B, WC, and CA states.

Fetch State (6)

A positive pulse at pulse amplifier output terminal PA28K sets a quadraflop to the F state. One of the following conditions triggers the pulse amplifier:

1. During power turnon, PWR CLR pulses arrive at terminal PA28L to directly trigger the pulse amplifier that sets the F state.

2. When the operator presses START, the KEY ST level conditions DCD level input PA28J (6, B1). The gate, triggered by special timing pulse SP1, causes the associated pulse amplifier to set the quadraflop to fetch.

3. During programmed operation, a ground F SET level conditions DCD level input PA28F when execution of an instruction is complete and there is no break request from an I/O device. Timing pulse T2B triggers the gate.

The F SET level generates at the output terminal PA30H of a 4-input NAND gate, when the gate is conditioned by $\overline{\text{B SET}}$, $\overline{\text{E SET}}$, $\overline{\text{D SET}}$, and $\overline{\text{SPEC CYCLE}}$ levels. These levels indicate that the next cycle is not required to be a break, execute, defer, or word count or current address cycle, respectively. The ground F SET level arrives at both the quadraflop setting pulse amplifier and the control logic gates. The control logic also requires a negative F SET level, which appears at inverter output terminal PB30D.

Execute State (6)

The E state is entered after the fetch cycle of a directly addressed memory reference instruction or after the defer cycle of an indirectly addressed memory reference instruction. A positive pulse at pulse amplifier output terminal PA28U sets the quadraflop to execute. The pulse amplifier is triggered by one of the following conditions:

1. During a manual examine or deposit operation, a ground KEY EX+DP level applied to terminal PA28R conditions a DCD input gate which special timing pulse SP1 triggers.

2. During programmed operation, a ground E SET level applied to terminal PA28T conditions a second DCD input gate which timing pulse T2B triggers.

A 3-input transistor NOR gate generates the E SET ground level when any of the following conditions exist:

1. A negative D(1) level from the quadraflop, indicating that the current cycle is a defer cycle, NAND combines with a negative $\overline{\text{JMP}}$ level, indicating that the current instruction is not a jump instruction. The ground E SET level appears at inverter output terminal PA30U.

2. Negative F(1), $\overline{\text{D SET}}$, $\overline{\text{JMP}}$, and $\overline{\text{IOT+OPR}}$ levels NAND combine and the ground E SET level appears at inverter output terminal PA31H. The F(1) level from the quadraflop indicates that the current cycle is a fetch; the $\overline{\text{D SET}}$ level indicates that the next cycle need not be a defer; the $\overline{\text{IOT+OPR}}$ level indicates that the current instruction is a memory reference instruction (neither an IOT nor an operate). This level is obtained by NAND combining the IR0 (1) and IR1 (1) output levels (operation codes of 6 or 7) from the instruction register flip-flops.

3. The negative KEY EX+DP level provides an enabling ground level to DCD gate at terminal PA28T from inverter output terminal PB33R. This level sets the E state to execute a TAD or a DCA instruction initiated by a manual examine or deposit operation.

Defer State (6)

The D state is entered after the fetch cycle of an indirectly addressed memory reference instruction. The quadraflop is set to the defer state when timing pulse T2B triggers a DCD input gate conditioned by a ground D SET level. The associated pulse amplifier then produces a pulse that sets the quadraflop to defer. The D SET level appears at NAND gate output terminal PA30N, when negative F(1), MB3 (1), $\overline{\text{INT ACK}}$, and $\overline{\text{IOT+OPR}}$ levels condition the gate. The F(1) level indicates that the current cycle is a fetch; the MB3 (1) level indicates that an indirectly addressed instruction is in progress; and the $\overline{\text{INT ACK}}$ level, generated in the program interrupt synchronization circuits, indicates that no interrupt request has been acknowledged. The $\overline{\text{IOT+OPR}}$ level was explained in the description of the execute state.

Break State (6)

The B state effects an information transfer between a high-speed I/O device and core memory during a data break. When a single-cycle data break occurs, the B state is entered after completion of the current instruction at the time of the request; after the fetch cycle in which a single-cycle augmented instruction has been completely executed; after the D cycle of a JMP instruction; or after any E cycle. A pulse appearing at terminal PA29M sets the quadraflop to break. The pulse generates when timing pulse T2B

triggers a DCD input gate conditioned by a complex gating circuit. This gate is conditioned when the CA(1) signal is negative (indicating that the second cycle of a 3-cycle data break is in progress), or when both the $\overline{\text{WC SET}}$ level is negative and the $\overline{\text{B SET}}$ level is at ground (indicating that a 1-cycle data break is to occur during the next cycle).

The B SET level appears at NAND gate output terminal PA31U when the negative $\overline{\text{E SET}}$ and $\overline{\text{D SET}}$ levels and a BRK SYNC (1) level condition the gate. Timing pulse T1 sets the BRK SYNC flip-flop in location PC32 whenever a high-speed I/O device, capable of using the break facility, applies a ground level BRK RQST signal to the DCD setting gate. The BRK RQST signal enters the processor interface at terminal PF3K. Timing pulse T2B clears the BRK SYNC flip-flop. The timing requirements of the BRK RQST and other data break signals supplied by the I/O device appear in Figures 2-2 through 2-5.

Word Count State (6)

The WC state, entered for the first cycle of a 3-cycle data break, occurs at T2 time when the WC SET level is at ground. The WC SET level is at ground when the CYCLE SELECT signal of the data break device is at ground and the $\overline{\text{B SET}}$ level is at ground. The CYCLE SELECT signal being at ground specifies that data breaks be 3-cycle breaks, and the $\overline{\text{B SET}}$ level being at ground indicates that a request has been made and conditions are ready to start a data break in the next cycle. Refer to the previous description of the break state for an explanation of the conditions that generate the $\overline{\text{B SET}}$ level.

Current Address State (6)

The CA state, entered at the end of the WC state of a 3-cycle data break, is set by a positive pulse from terminal PD05M. The WC(1) ground level enables the pulse amplifier producing this pulse. Therefore, the CA state can only be entered following the WC state, and no other state can be entered from the WC state.

Distribution of Major State Signals (6, 10)

The six major state negative levels F, E, D, B, WC, and CA are used extensively for gating purposes in the processor control logic circuits as are the ground level SET signals and the negative $\overline{\text{SET}}$ levels. Note that for a given SET level to appear, only one group of conditions must be completely satisfied. The ground level which appears at the output of the gate associated with that group then overrides negative levels produced by other incompletely fulfilled condition groups. Thus, if some conditions are met, but no group of conditions is completely satisfied, a negatvie $\overline{\text{SET}}$ level replaces the ground SET level at the input of the associated DCD gate, and no setting pulse is produced for that state.

A negative buffered B level, designated B BREAK, flows to high-speed devices using the data-break facility. The ground B level which appears at terminal PB25L of the quadraflop flows to bus driver VT in module PE8 (10, B5). The Type R650 Bus Driver module, which can drive a 20-ma load, has both inverting and noninverting inputs. This application uses the inverting input (terminal PE8V). The negative B BREAK level from output terminal T flows to interface terminal PF3P.

PROGRAM COUNTER CONTROL (8)

PC control generates command pulses required for clearing all or part of the PC, loading the PC from the SWITCH REGISTER, loading all or part of the PC from the MB, and incrementing the contents of the PC. The logic circuits of the PC control appear at the right of engineering drawing 8.

Clearing and Loading Operations

The program counter register has two sections for clearing and loading purposes. Bits PC0 through PC4 specify the memory page of the next instruction, and these bits may be cleared and loaded separately. Bits PC5 through PC11 specify a location within a memory page.

Clearing Pulses

The clearing pulses are designated 0 ⟶ PC0-4, and 0 ⟶ PC5-11. The 0 ⟶ PC0-4 pulse generates from the pulse amplifier circuit PMN of the Type S603 module in location PC23 (8, A6). During the fetch cycle of a JMP or JMS instruction, the pulse amplifier DCD input gate is conditioned by NAND combining the F level from the major state generator, an MB3 (0) level signifying that the instruction is directly addressed, MB4 (0) level signifying that the jump is to be made to a location in memory page 0, and the JMP+JMS level. Timing pulse T2B then triggers the DCD gate and the 0 ⟶ PC0-5 pulse appears at terminal PC23M. A 0 ⟶ PC5-11 pulse also triggers the pulse amplifier.

The 0 ⟶ PC5-11 pulse generates from pulse amplifier circuit EHLK of the Type S602 module in location PD22. The pulse amplifier is triggered by any of the following conditions:

1. During a manual load address operation, a ground KEY LOAD ADDRESS level, conditions DCD gate HJ and special timing pulse SP1 triggers it.

2. When a program interrupt initiates, the ground INT ACK level conditions DCD gate EF, and timing pulse T2B triggers it.

3. At the end of a power interruption, the PC CLEAR pulse from the KR01 Automatic Restart option triggers the PA to set address 0 for the first instruction.

The 0 ⟶ PC5-11 pulse appears at terminal PD22K and not only flows to the clear inputs of the register flip-flops, but also to the diode input of the 0 ⟶ PC0-4 generator. Thus, whenever bits PC5-11 clear, bits PC0-4 automatically clear also. The 0 ⟶ PC5-11 pulse arrives at interchassis cable terminal PD2F for use in the memory extension control.

Loading Pulses

The three loading pulses are designated SR ⟶ PC, MB ⟶J⟶ PC0-4, and MB ⟶J⟶ PC5-11. During manual operations, the SR ⟶ PC pulse effects a transfer of binary 1's from the SWITCH REGISTER into corresponding bits of the PC. This pulse generates from pulse amplifier circuit DFH in the Type S603 module in location PC23. DCD gate DE, conditioned by a ground KEY LOAD ADDRESS level from the key circuits, is triggered by special timing pulse T2B. The SR ⟶ PC positive pulse appears at terminal PC23F and goes to the register input gates. The SR ⟶ PC pulse also arrives at interchassis connector terminal PD2D for use in the memory extension control.

During programmed operation, information may jam-transfer into the PC from the corresponding bits of the MB. For jam-loading, as for clearing, the PC is divided into two sections of bits PC0-4 and bits PC5-11. The relationship between sections is the opposite of that in clearing operations, whereas bits PC0-4 can be cleared independently of bits PC5-11 and bits PC5-11 can be loaded independently of bits PC0-4.

Pulse amplifier circuit VTU in the Type S603 module at location PD20 generates the MB ⟶J⟶ PC5-11 pulse. An MB ⟶J⟶ PC5-11 ENABLE ground level conditions the DCD input gate of this pulse amplifier and timing pulse T2B triggers it. The enabling level is generated during the fetch cycle of a directly addressed JMP or JMS instruction by NAND combining the F, MB3 (0), JMP+JMS, and $\overline{\text{INT ACK}}$ negative levels. The MB ⟶J⟶ PC5-11 ENABLE level appears at NAND gate output terminal PC27U, and is available at interchassis connector terminal PD2E for use in the memory extension control. The MB ⟶J⟶ PC5-11 pulse is also generated whenever an MB ⟶J⟶ PC0-4 pulse appears at pulse amplifier input terminal PD20V.

The MB ⟶J⟶ PC0-4 pulse generates during the defer cycle of an indirectly addressed JMP or JMS instruction. DCD gate KL of module PD20, conditioned by an MB ⟶J⟶ PC0-4 ENABLE level, is triggered by timing pulse T2B. The MB ⟶J⟶ PC0-4 pulse, from pulse amplifier output terminal PD20M, goes to the register and to the diode input terminal PD20V of the MB ⟶J⟶ PC5-11 generator. The MB ⟶J⟶ PC0-5 ENABLE level occurs by NAND combining the negative D and JMP+JMS levels. The enabling level arrives at interchassis connector terminal PD2R for use in the memory extension control.

Incrementing Operations

The contents of the PC increment at the beginning of each fetch cycle, so that when the current instruction is executed the processor can proceed to the next instruction. The contents of the PC also increment at other times so that the program count can, under certain conditions, advance by one or two instructions. In general, conditions that cause the contents of the PC to increment can be divided into two groups: those associated with instructions of the operate or IOT classes, and those associated with memory reference instructions or manual operations. Both a positive COUNT PC pulse which complements flip-flop PC11, and a PC CARRY command pulse which propagates carries toward bit PC0 perform incrementation. The COUNT PC and PC CARRY commands, when used together, increment the contents of the PC by 1. During operate instructions, if skip conditions are satisfied, the COUNT PC pulse is suppressed; and the PC CARRY pulse is generated alone. This pulse complements bit PC10, incrementing the contents of the PC by 2 and causing the next instruction to be skipped.

Incrementing by 1

The COUNT PC pulse complements flip-flop PC11 and, if this flip-flop already contains a 1, causes generation of a PC CARRY pulse which complements flip-flop PC10 and propagates any carries required. Thus, the contents of the PC increment by 1. The COUNT PC pulse generates under the following conditions:

1. During a manual examine or deposit operation, negative NAND gate DEH in module PC28 (8, D5), conditioned by a negative KEY EX+DP level from the key circuits, is enabled by special timing pulse SP1. The positive pulse which appears at terminal PC28H arrives at the diode input of pulse amplifier circuit VUN in module PD22. The COUNT PC pulse appears at terminal PD22U. This incrementation allows examine and deposit operations to occur at successive core memory locations without manually specifying each address.

2. During the fetch cycle of memory reference instructions other than JMP or JMS, negative F(1), $\overline{\text{JMP}}$, $\overline{\text{JMS}}$, and $\overline{\text{OP SKIP}}$ levels condition negative NAND gate KLMN in module PC28 (8, D6). Timing pulse T1 enables the gate, and the positive pulse appearing at terminal PC28N generates the COUNT PC pulse. This operation is the standard means of stepping the processor through a sequence of instructions at consecutive core memory addresses.

3. During the execute cycle of an ISZ instruction, negative NAND gate NTU of module PC28 is conditioned by the E(1) level from the major state generator, the ISZ level from the IR decoder, the TG (1) level from the timing generator, and the RUN(1) level from the run control during time state T1. The ground level which appears at terminal PC28U conditions DCD input gate ST of the COUNT PC ganerator. The MB is loaded and increments by 1; if the incrementation sets the MB to 0, indicated by bit MB0 changing from 1 to 0, the MB0 (0) transition triggers the DCD gate, generating a COUNT PC. This action causes the processor to skip the next instruction.

4. During the execute cycle of a JMS instruction, the negative JMS level from the IR decoder inverts and conditions DCD input gate PR of the COUNT PC generator. Timing pulse T1E triggers this gate generating a COUNT PC.

5. A +1 ⟶ PC ENABLE level generated by the 182 Extended Arithmetic Element enables DCD gate PR of the COUNT PC generator. This input increments the program count with the T1E pulse during a multiply instruction to locate the multiplier or during a divide instruction to locate the divisor in the core memory location following the instruction.

6. The PC COUNT ENABLE pulse at terminal PB21T (10, C8) goes directly to the diode input of the pulse amplifier, causing generation of a COUNT PC pulse.

The COUNT ENABLE pulse generates externally in the KR01 Automatic Restart option, and internally from pulse amplifier RSVTU in PB21. This pulse amplifier is triggered by either of the following means:

1. A positive SKIP pulse supplied to the SKIP BUS IN interface terminal PF02K triggers the pulse amplifier during satisifed IOT skip instructions.

2. The T2E pulse when enabled by the ground TT SET level triggers the input DCD gate, indicating that the 681 Data Line Interface option is executing an instruction.

Incrementing by 2

The PC CARRY pulse complements flip-flop PC10 during satisfied OPR 2 skip instructions. If this flip-flop already contains a 1, the PC CARRY pulse complements flip-flop PC9 also and propagates similar carries, as required, toward flip-flop PC0. The PC CARRY pulse is generated by the following conditions:

1. A carry from bit PC11 is required, when, after incrementing the contents of the PC by 1, the DCD input gate DE of module PD20 (8, A6) is conditioned by the PC11 (1) level, indicating that the COUNT PC pulse will condition this flip-flop, thus requiring a carry. Storage time of the DCD gate allows it to be triggered by the COUNT PC pulse, so the output of the gate triggers pulse amplifier circuit JFH in module PD22, and the PC CARRY pulse appears at terminal PD20F.

2. When the contents of the PC are to increment by 2, negative NAND gate KLN in module PC26 is conditioned by an OP SKIP level and is triggered by timing pulse T1. The positive pulse which appears at terminal PC26N arrives at the diode input of the PC CARRY generator, and the PC CARRY pulse appears at terminal PD20F. This pulse complements flip-flop PC10 and propagates any required carries. Since the state of flip-flop PC11 remains unchanged, the generation of a PC CARRY pulse alone effectively increments the contents of the PC by 2, causing the processor to skip the next instruction.

Instruction bits in MB5 through MB8 and conditions in the AC and/or link produce the OP SKIP level. The circuits which produce the OP SKIP level appear in zones C5 through C8 of engineering drawing 8. These circuits consist of a large OR gate with each input provided by an AND gate that senses a bit of the instruction and applicable conditions of the AC and L, producing a skip when the conditions are satisfied. Typical skip conditions are:

1. NAND gate KLMN of module PD27 and the associated diodes of module PD29 (8, C5, D5) sense the zero or nonzero state of the AC. The 0 levels of bits AC0 through AC11 combine with the MB6 (1) level (designating the SZA instruction) in this gate. The gate produces a negative level at output terminal PD27N if the contents of the AC are not 0 and a ground level is the contents of the AC are 0.

2. NAND gate RSU of module PD27 senses the positive or negative sign of the binary number in the AC. The AC0 (1) level combines with the MB5 (1) level (designating the SMA instruction), and the gate produces a ground level at output terminal PD27U, indicating that the sign of the AC is negative. For a positive sign, this gate produces a negative output level.

3. NAND gate DEH of module PD27 senses the contents of the link. The L (1) level combines with the MB7 (1) level (designating the SNL instruction) and the gate produces a ground level at output terminal PD27H, indicating that the contents of the link are 1. When the link contains a 0, the gate gives a negative output level.

The OP SKIP level appears at output terminals PD28N and PD28U of two NAND gates which sense the status of bit MB8. These gates sense the condition of the bit 8 of the instruction and serve as a reversing switch that enables skipping on the normal condition when MB8 (0) or skipping on the inverse conditions when MB8 (1).

MEMORY ADDRESS REGISTER CONTROL (8)

The MA control generates the command pulses required for clearing all or part of the MA; loading all or part of the MA from the corresponding bits of the MB; jam-transferring the contents of the PC into the MA; and jam-transferring into the MA information supplied by the twelve address lines of a high-speed I/O device using the data break facility.

The memory address register has two parts for clearing and loading purposes. Bits MA0 through MA4 specify the memory page of an instruction or operand; bits MA5 through MA11 specify the location of a given cell within that page. During clearing operations, bits MA0 through MA4 may be cleared independently; however, any pulse which clears bits MA5 through MA11 also clears bits MA0 through MA4. During loading operations, a jam-transfer from the corresponding bits of the MB may load bits MA5 through MA11; however, any pulse which causes a jam-transfer from the MB into bits MB0 through MA4 also causes a jam-transfer into bits MA5 through MA11.

Clearing Pulses

The clearing pulses are designated 0 ⟶ MA0-4 and 0 ⟶ MA5-11. Pulse amplifier circuit PMN in the Type S603 module at location PC21 generates the 0 ⟶ MA0-4 pulse. DCD gate KL of this pulse amplifier is conditioned during the fetch cycle of a memory reference instruction that addresses a cell in page 0 of memory. Timing pulse T2B triggers the gate; the 0 ⟶ MA0-4 pulse appears at terminal PC21M and clears bits MA0 through MA4.

The conditioning level is obtained from NAND gate output terminal PC25H, which produces a ground level when the four inputs of the gate are conditioned by negative F(1) and $\overline{\text{B SET}}$ levels from the major state generator, a $\overline{\text{IOT+OPR}}$ level from the instruction register, and an MB4 (0) level indicating an address in page 0.

Pulse amplifier circuit DFH in the Type S603 module at location PC21 generates the 0 ⟶ MA5-11 pulse. An INT ACK ground level conditions DCD gate DE of this pulse amplifier, indicating that a program interrupt request has been acknowledged, and timing pulse T2B triggers the gate. The 0 ⟶ MA5-11 pulse appears at terminal PC21F. This pulse clears bits MA5 through MA11 and flows to the diode input of the 0 ⟶ MA0-4 generator, so that bits MA0 through MA4 are cleared also. Being cleared, the MA specifies core memory address 0000 which stores the program count during a program interrupt.

Loading Pulses

There are four loading pulses, designated MB —J→ MA0-4, MB —J→ MA5-11, PC —J→ MA, and DATA ADD —J→ MA. The MB —J→ MA5-11 pulse generates during the fetch cycle of a memory reference instruction from pulse amplifier circuit PMN of the S603 module at location PC22. The DCD input gate, conditioned by a ground level obtained from NAND gate output terminal PC26H, is triggered by timing pulse T2B. The MB —J→ MA5-11 pulse appears at terminal PC22M. The NAND gate produces a ground level output when the four inputs of the gate are conditioned by negative F(1) and $\overline{\text{B SET}}$ levels from the major state generator, a $\overline{\text{INT ACK}}$ level from the program interrupt synchronization circuits, and a $\overline{\text{IOT+OPR}}$ level from the instruction register. In other words, the MB —J→ MB5-11 pulse generates during the fetch cycle of a memory reference instruction.

Pulse amplifier circuit DFH in module PC22 generates the MB —J→ MA0-4 pulse during the defer cycle of any indirectly addressed memory reference instruction. DCD input gate DE, conditioned by a ground level obtained from NAND gate output terminal PC25U, is triggered by timing pulse T2B. The NAND gate gives a ground level output when its two inputs are conditioned by negative D(1) and $\overline{\text{B SET}}$ levels from the major state generator. The MB —J→ MA0-4 pulse appears at terminal PC22F and flows to the MA input gates and to the diode input of the MB —J→ MA5-11 generator. Thus, whenever bits MA0 through MA4 are loaded from the MB, an additional pulse generates that causes bits MA5 through MA11 to be loaded also.

Pulse amplifier circuit HEK of the S602 module at location PC20 generates the PC —J→ MA pulse. This pulse occurs under the following conditions:

1. During a manual start, examine, or deposit operation, a ground KEY ST+EX+DP level conditions DCD gate EF, which is triggered by special timing pulse SP1. The PC —J→ MA pulse appears at terminal PC20K. This operation transfers the address into the MA from the PC which was loaded previously from the SWITCH REGISTER.

2. During the fetch cycle of an OPR or IOT instruction when there is no break request, a ground PC ——→ MA ENABLE level conditions DCD gate HJ, which is triggered by timing pulse T2B. The PC ——→ MA ENABLE level comes from NAND gate output terminal PC25N when the two inputs of the gate are conditioned by a negative F SET level from the major state generator and a negative $\overline{\text{JMP}}$ level from the IR decoder.

3. During the execute cycle of any memory reference instruction (except JMP which has no execute cycle) when there is no break request, the pulse generates as described in 2.

Pulse amplifier circuit RSTU in module PC22 generates the DATA ADD —J—▶ MA pulse at the end of any cycle immediately preceding a break cycle. As soon as a break request is granted, the major state generator generates a B SET level. This level is strobed into the quadraflop by the T2B pulse, establishing the B or WC state for the next cycle. The B SET level also conditions DCD input gate in module PC22. Timing pulse T2B triggers the gate, and the DATA ADD —J—▶ MA pulse appears at terminal PC22T. This pulse strobes the information supplied by the data address lines into the MA. In addition, the DATA ADD —J—▶ MA pulse goes to pulse amplifier circuit DHJ in module PF10 (10, B7). This pulse amplifier produces an ADDRESS ACCEPTED pulse at terminal PF10H, which flows to interface connector terminal PF3S for use in the high-speed I/O device using the data break facility.

MEMORY BUFFER REGISTER CONTROL (5)

The logic circuits of the MB control are shown along the lower portion of engineering drawing 5. Five command pulses are generated and are designated 0 ——▶ MB, COUNT MB, AC ——▶ MB, PC —J—▶ MB, and DATA ——▶ MB.

Pulse amplifier circuit PVUN in the Type S602 module at location PC20 generates the 0 ——▶ MB pulse. The pulse appears at output terminal PC20U and generates under the following conditions:

1. During a manual start, examine, or deposit operation, DCD gate ST of module PC20, conditioned by a ground KEY ST+DP+EX level, is triggered by special timing pulse SP1.

2. During an ADC instruction (analog-to-digital conversion), the T1 pulse generates an IOT 004 pulse which flows to the diode input of the 0 ——▶ MB generator.

3. During time state T2 of every computer cycle except those listed below, a ground level from inverter HF in module PD26 conditions DCD gate PR of module PC20, which is triggered by timing pulse T2B. Note, however, that this inverter produces a negative level that inhibits the gate under the following conditions:

   a. During the fetch cycle of a directly addressed JMS instruction, negative F(1), JMS, and MB3 (0) levels combine in NAND gate RSTU of module PD23, and the ground level appearing at terminal PD23U inverts to inhibit the DCD gate.

   b. During the defer cycle of an indirectly addressed JMS instruction, negative D(1) and JMS levels combine in NAND gate KLN of module PD23, and the ground level appearing at terminal PD23N inverts to inhibit the DCD gate.

c. When a program interrupt is granted, the negative INT ACK level from the program interrupt synchronization circuits inverts in module PD26 to inhibit the DCD gate.

The COUNT MB pulse, which increments the contents of the MB by 1, generates from pulse amplifier circuit RSTU in the Type S603 module at location PC21. The pulse appears at terminal PC21T and generates under the following conditions:

1. A+1 ⟶ MB (or INCREMENT MB) ground level originating in external equipment flows to interface connector terminal PF03T. The ground level (inverted twice in module PD31 for isolation purposes) conditions DCD gate RS of module PC21 which is triggered by timing pulse T1.

2. During the execute cycle of an ISZ instruction, negative E(1) and ISZ levels combine in NAND gate RSU of module PD24; the gate produces a ground level to condition the DCD gate of the count MB generator.

3. During the execute cycle of a JMS instruction that is not the result of a program interrupt acknowledgement, negative E(1), JMS, and $\overline{\text{INT ACK}}$ levels combine in NAND gate KLMN of module PD24; the gate produces a ground level at terminal PD24N to condition the DCD gate of the count MB generator.

4. During the defer cycle of an autoindexing operation, when an instruction contains a 1 in bit MB3 and specifies one of the locations 10_8 through 17_8 in page 0 of memory, the contents of that location are read, incremented by 1, and act as the effective address of the instruction. The D(1) level from the major state generator combines with negative levels denoting MA0 (0) through MA7 (0) and MA8 (1) in NAND gate DEFH of module PD25. The ground level produced at terminal PD25H conditions the DCD gate of the count MB generator.

5. During the word count state of a three-cycle data break, the WC (1) negative level at terminal M of the S107 module at PE07 provides a ground enabling level to the input gate of the count MB generator. The COUNT MB pulse which generates under these conditions increments the word count.

6. During the current address state of a three-cycle data break, the CA (1) negative level from the major state generator and the +1 ⟶ CA INHIBIT negative level from the transferring device NAND combine in gate DEF of module PE10. If the +1 ⟶ CA

level at interface connector PF04M is negative, the NAND gate enables the input gate of the count MB generator. The COUNT MB pulse which generates under these conditions increments the address of the data break transfer.

7. At time T1 of the status state of a TTI instruction, the 681 Data Line Interface option produces a positive COUNT MB ENABLE pulse that directly triggers the count MB generator. COUNT MB pulse which generates under these conditions increments the status word.

Pulse amplifier circuits KNF in the Type W640 module at location PF10 (10, D7) generates the WC OVERFLOW pulse. This negative 400-nsec pulse flows to the device using the 3-cycle data break from interface connector PF04P. This pulse generates during the word count state of a data break if the word count becomes 0 when it is incremented. The pulse serves as a flag to the I/O device, indicating that the current data break should be the last one until some address modification is made. The WC (1), TG (1), and RUN (1) negative levels combine the diode gate RSTU at location PE10 to condition the input DCD gate of pulse amplifier circuit RSTU of the Type S603 module at PD05. The gate, conditioned when the timing generators are enabled and are in the T1 time state of a WC major state, produces the WC OVERFLOW pulse by changing the most significant bit of the MB from 1 to 0. This change can occur only when the word count changes from the full count to a 0 count when incremented.

Pulse amplifier circuit KLMN in the Type S603 module at location PD21 generates the AC ⟶ MB pulse. A DCA level from the IR decoder conditions the DCD input gate of this pulse amplifier and timing pulse T1E triggers it. Thus, the AC ⟶ MB pulse occurs only in time state T1 during the execute cycle of a DCA instruction.

The PC ⟶ MB pulse generates from the pulse amplifier circuit RSTU in the Type S603 module at location PD21. The conditions which cause generation of this pulse are identical with those which cause inhibition of the 0 ⟶ MB pulse, except that the PC ⟶ MB pulse is not generated when manual keys are operated.

The DATA ⟶ MB pulse generates from pulse amplifier circuit DEFH of the Type S603 module at location PD21. This pulse occurs only during time state T1 in a break cycle requested for an inward information transfer. The negative DATA IN level (transfer direction in signal) supplied by the I/O device requesting the break enters the processor at interface connector terminal PF3M. The DATA IN level combines with the B (1) level in NAND gate DEH of module PD23. The ground level at terminal PD23H conditions the DCD gate of the DATA ⟶ MB generator, which is triggered by timing pulse T1E.

ACCUMULATOR REGISTER AND LINK CONTROL (3)

The AC control generates command pulses for clearing, rotating, and complementing the contents of the AC and link, and for transferring information into these registers. The AC and link can be cleared, complemented, and set to all 1's independently of each other; however, in all rotate operations the link functions as an extension of the AC. In the following paragraphs, command pulses pertaining to the AC are described first; descriptions of pulses pertaining to the link follow; finally, pulses which affect both AC and link are described.

AC Command Pulses

Clear AC

The 0 ⟶ AC (clear AC) pulse generates at pulse amplifier circuit SPVUN of the Type S602 module at location PA20 and simultaneously resets all bits of the accumulator register to 0. The 0 ⟶ AC pulse appears at terminal PA20U (3, B7) and generates under the following conditions:

1. During a manual start, examine, or deposit operation, a KEY ST+EX+DP level conditions DCD gate ST in module PA20 and special timing pulse SP1 triggers it.

2. During the execute cycle of a DCA instruction, the DCA level from the IR decoder conditions DCD input gate PR of module PA20 and timing pulse T1E triggers it.

3. When a Group 1 OPR instruction contains a CLA microinstruction but not a CMA microinstruction (MB4 = 1 and MB6 = 0), NAND gate KLMN in module PA25 is conditioned by OPR, F(1), and MB4(1) levels and by a negative level from output terminal PB23U of a second NAND gate (RSU in module PB23) when the latter is disabled. The NAND gate in module PA25 is enabled by timing Pulse T1 and the ground level appearing at terminal PA25N generates the 0 ⟶ AC pulse. Note that if a Group 1 OPR instruction contains both CLA and CMA microinstructions, whose combined effect is to set all bits of the AC to 1, the NAND gate in module PB23 is enabled by the OP1 and MB6(1) levels. The ground level at terminal PB23U inhibits the NAND gate in module PA25, suppressing the 0 ⟶ AC pulse. Under these conditions, the AC is set to all 1's by the 1 ⟶ AC pulse.

4. During a Group 2 OPR instruction containing a CLA microinstruction (MB4 = 1), the above levels condition the NAND gate KLMN in module PA25. The absence of the

OP1 level now disables NAND gate RSU in module PB23; therefore, a negative level appears at terminal PB23U and permits timing pulse T1 to enable the NAND gate in module PA25 and generates the 0 ⟶ AC pulse.

5. During an ADC instruction, an IOT 004 pulse generates at T1 and flows to the 0 ⟶ AC generator through OR gate LMN of module PA26 (3, B5).

6. An AC ⟶ MQ command from the EAE arrives at the 0 ⟶ AC generator through OR gate LMN in module PA26.

7. During a KCC instruction, an IOT 032 pulse generates at event time 2 of the pause. This pulse, originating in the keyboard device selector, enters the processor through terminal S of the interchassis connectors at locations MD35 and PD2 and triggers pulse amplifier circuit DEJFH in the S603 module at location PA19. The output of the pulse amplifier appears at terminal PA19F and triggers the 0 ⟶ AC generator.

8. When a positive pulse reaches the CLEAR AC line that enters the processor at terminal P of the in/out connector at location PF2, the positive pulse flows to the diode input of pulse amplifier DEFJH in module PA19. The output of this pulse amplifier triggers the 0 ⟶ AC generator.

Set Accumulator

The 1 ⟶ AC pulse generates from a Group 1 OPR instruction microprogrammed for both CLA and CMA instructions. NAND gate RSTU in module PA25 is conditioned by negative MB4 (1), MB6 (1), and OP1 levels, denoting CLA and CMA microinstructions and an operate instruction, respectively. Timing pulse T1 enables the gate and the positive pulse at terminal PA25U flows to the direct set inputs of all bits of the AC, setting them to 1.

Complement Accumulator

The COMP ⟶ AC pulse generates at the output terminal of inverter VT in module PA21 (3, A7). This pulse occurs when an EAE COMP AC pulse arrives at the inverter input terminal or when a Group 1 OPR instruction contains a CMA microinstruction (MB6 = 1) but no CLA microinstruction (MB4 = 0). NAND gate DEFH of module PA25 is conditioned by MB4 (0), MB6 (1), and OP1 levels and is enabled by timing pulse T1. The positive pulse at terminal PA25H inverts and flows to the complementing input gates of the AC so that all bits complement.

Transfer MB 0's to Accumulator

The MB $\xrightarrow{0}$ AC pulse generates at pulse amplifier RSTU in the Type S603 module at location PB19. The pulse appears at terminal PB19T and generates during the execute cycle of a logical AND instruction. The AND level from the IR decoder conditions the DCD input gate of the pulse amplifier, and the gate is triggered by timing pulse T2E. The MB $\xrightarrow{0}$ AC pulse clears to 0 those flip-flops of the AC corresponding to MB flip-flops in the 0 state.

Switch Register to Accumulator

The SR $\longrightarrow$ AC pulse generates at pulse amplifier circuit EHK of the S602 module at location PB20. This pulse causes a transfer of binary 1's from the SWITCH REGISTER into the AC, and occurs under the following conditions:

1. During a manual deposit operation, DCD gate EF, conditioned by a KEY DP level from the key circuits, is triggered by special timing pulse SP2. The SR $\longrightarrow$ AC pulse appears at terminal PB20K.

2. During a Group 2 OPR instruction containing an OSR microinstruction (MB9 = 1), the OP2 and MB9 (1) levels combine in NAND gate KLN of module PB23. The ground level appearing at terminal PB23N conditions DCD gate HJ which is triggered by timing pulse T2A. The resulting SR $\longrightarrow$ AC pulse transfers binary 1's from the SWITCH REGISTER to the AC, and the final contents of the AC are the inclusive OR of 1's originally stored in the AC or transferred from the SR.

Half Add

The HALF ADD pulse generates from pulse amplifier circuit KPMN in the Type S603 module at location PB21. This pulse occurs under the following conditions:

1. During an EAE addition, an EAE HALF ADD pulse arrives at the diode input of the half add generator. The HALF ADD pulse appears at terminal P21M and causes MB flip-flops in the 1 state to complement the corresponding bits of the AC. A CARRY pulse completes addition.

2. During the execute cycle of a TAD instruction, a TAD level from the IR decoder conditions DCD input gate KL which is triggered by timing pulse T1E. The HALF ADD pulse performs as in paragraph 1. A CARRY pulse propagates 1's to complete the 2's complement addition.

Link Command Pulses

Clear Link

The 0 ⟶ L pulse flows to a direct clear input of the link and resets this flip-flop to 0. The 0 ⟶ L pulse generates under the following conditions:

1. During a manual start operation, NAND gate KLN in module PA24 is conditioned by a negative KEY ST level from the key circuits and is enabled by special timing pulse SP1. The 0 ⟶ L pulse appears at terminal PA24N.

2. During execution of a Group 1 OPR instruction containing a CLL microinstruction but not a CML microinstruction, NAND gate KLMN in module PA22 is conditioned by OP1, MB5 (1), and MB7 (0) levels and is enabled by timing pulse T1. The 0 ⟶ L pulse appears at terminal PA22N.

Complement Link

The COMP ⟶ LINK pulse generates during execution of a Group 1 OPR instruction containing a CML microinstruction but not a CLL microinstruction. NAND gate DEFH in module PA24 is conditioned by OP1, MB5 (0), and MB7 (1) levels and is enabled by timing pulse T1. The positive COMP ⟶ LINK pulse appears at terminal PA24H.

Set Link

The 1 ⟶ L pulse generates during execution of a Group 1 OPR instruction containing both CLL and CML microinstructions. NAND gate RSTU of module PA24 is conditioned by OP1, MB5 (1) and MB7 (1) levels and is enabled by timing pulse T1. The positive 1 ⟶ L pulse at terminal PA24U flows to a direct set input of the link and sets this flip-flop to 1.

Combined AC and Link Command Pulses

Group 1 and Group 2 Identifiers

Group 1 OPR instructions have a 0 in bit 3 of the instruction word and produce an OP1 level and a POP1 pulse for gating the AC control logic. Group 2 OPR instructions are identified by a 1 in bit 3 and a 0 in bit 11 of the instruction word and produce an OP2 level for gating purposes.

Negative and ground OP1 levels are generated by combining negative F (1), OPR, and MB3 (0) levels in NAND gate DEFH of module PA22. The ground OP1 level at terminal PA22H (3, A1) inverts to produce the negative OP1 level at terminal PA21D (3, A2).

The POP1 pulse (possible overflow pulse), used for producing rotate command pulses, is obtained by conditioning the DCD input of pulse amplifier DEFH in module PB21 with the OP1 level (3, B1). Timing pulse T2A triggers the DCD gate, and the POP1 pulse appears at pulse amplifier output terminal PB21F.

Negative and ground OP2 levels generate by combining negative F (1), OPR, MB3 (1), and MB11 (0) levels in NAND gate RSTU of module PA22. The ground OP2 level at terminal PA22U inverts to produce the negative OP2 level at terminal PA21F.

Carry

The CARRY pulse generates at pulse amplifier circuit EHLK in the Type S602 module at location PA20 and flows to the carry gates at the complement inputs of the AC flip-flops to produce required carries after a half-add operation. The CARRY pulse generates under the following conditions:

1. An EAE CARRY pulse flows to the diode input of the carry generator during an EAE addition. The CARRY pulse appears at terminal PA20K.

2. During the execute cycle of a TAD instruction, DCD input gate HJ, conditioned by the TAD level from the IR decoder, is triggered by timing pulse T2E.

3. During a Group 1 OPR instruction containing an IAC microinstruction (bit MB11 = 1), DCD input gate EF, conditioned by the MB11 (1) level, is triggered by a POP1 pulse during time state T2.

Rotate Command Pulses

The RAR pulse generates at pulse amplifier circuit KPMN in the Type S603 module at location PA19. The pulse appears at terminal PA19M when an MQ SHIFT RIGHT pulse from the EAE arrives at the diode input of the pulse amplifier or during a Group 1 OPR instruction containing a 1 in bit 8. The MB8 (1) and MB10 (0) levels combine in NAND gate DEH of module PB22, and the ground level at terminal PB22H conditions DCD gate KL of the RAR generator. A POP1 pulse triggers the DCD gate during time state T2.

The RTR pulse generates at pulse amplifier KLMN of the Type S603 module at location PB19. The DCD gate is conditioned by combining the MB8 (1) and MB10 (1) levels to produce a ground level at terminal PB22N. A POP1 pulse triggers the gate during time state T2. The RTR pulse appears at terminal PB19M.

The RAL pulse generates at pulse amplifier circuit RSVTU of the Type S603 module at location PA19. The pulse appears at terminal PA19T when an EAE AC ROTATE LEFT pulse arrives at the diode input of the RAL generator or during execution of a Group 1 OPR instruction containing a 1 in bit 9. The MB9 (1) and MB10 (0) levels NAND combine, producing a ground level at terminal PB22U which conditions DCD gate RS. A POP1 pulse triggers this gate during time state T2.

The RTL pulse generates at pulse amplifier circuit DEFH of the Type S603 module at location PB19. The DCD gate is conditioned by NAND combining the MB9 (1) and MB10 (1) levels to produce a ground level at terminal PB23H. During time state T2 a POP1 pulse triggers the DCD gate, and the RTL pulse appears at terminal PB19F.

PROGRAM COUNTER, MEMORY ADDRESS, AND MEMORY BUFFER REGISTERS (4, 8, 16)

The program counter, memory address, and memory buffer registers utilize double-height Type R211 modules at locations PC7/PD7 through PC18/PD18. Each Type R211 module contains one bit of the PC and the corresponding bits of the MA and MB.

Program Counter Register (4)

Each bit of the PC contains four DCD gates and a direct clear input. One DCD gate in each bit connects to the set input and is conditioned by a binary 1 in the corresponding bit of the SWITCH REGISTER. The SR ⟶ PC command pulse triggers all these gates simultaneously and effects a transfer of 1's from the SWITCH REGISTER to the PC.

One DCD gate in each bit connects to the complement input and is conditioned when all bits of less significance (down to bit PC10) are in the 1 state. The COUNT PC pulse from PC control triggers the complement DCD gate of bit PC11. The PC CARRY pulse from the PC control triggers the complement DCD gates of all other PC flip-flops.

The remaining two DCD gates connect to the (1) and (0) inputs of the flip-flop respectively. The gates are conditioned by the (1) and (0) levels of the corresponding MB bit. Both gates are triggered simultaneously by the MB ⟶J⟶ PC command pulse from the PC control and jam-transfer information from the MB into the PC. Note that for clearing and jam-transferring, the PC flip-flops are divided into two groups: PC0 through PC4 and PC5 through PC11. The PC flip-flops are unbuffered and drive a 15-ma load at ground from either terminal.

Memory Address Register (4)

Each bit of the memory address register contains a direct clear input and three pairs of DCD gates for jam-transferring. One pair of DCD gates is conditioned by the (1) and (0) levels of the corresponding bit of the MB; the second pair is conditioned by the corresponding bit of the PC; the third pair is conditioned by the corresponding data address line of a high-speed I/O device using the data break facility. The data address line provides a ground level corresponding to a binary 1, and this arrives directly at the MA (1) DCD gate. The negative level corresponding to a binary 0 flows to the (0) DCD gate through an inverter which is an integral part of the Type R211 module.

Like the PC, the MA is divided into two sections: bits MA0 through MA4 and bits MA5 through MA11. The MA control provides separate pulses for each section when the MA is to be cleared or loaded from the MB. When the MA is to be loaded from the PC or from the data address lines, all MA flip-flops are set simultaneously. The MA flip-flops are buffered and drive a 25-ma load at −3v and a 7-ma load at ground.

Memory Buffer Register (5, 16)

Each bit of the MB register contains a direct clear input, a complement input, a direct set input, two DCD set inputs, and two pairs of DCD gates for jam-transferring.

Direct Clear Input

The flip-flops of the MB are cleared collectively by a 0 ⟶ MB command pulse supplied by the MB control.

Complement Input

The contents of the MB increment by 1 when a COUNT MB command pulse from the MB control arrives at the DCD input gates of the complement input. The complementing input of bit MB11 is permanently conditioned by a ground applied to the DCD gate. Thus, each time the COUNT MB pulse generates, bit MB11 complements. The other bits are conditioned when all bits of less significance are in the 1 state. Thus, if bits MB7 through MB11 are in the 1 state, a COUNT MB pulse sets these bits to 0 and complements bit MB6.

Direct Set Input

The direct set input at terminal CT of each module connects to the sense amplifier outputs of the memory system. The direct set input is ungated; therefore, if it is necessary to retain the contents of the MB

during time state T2 (as in the execute cycle of a JMS instruction), the memory strobe pulse must be suppressed. Under these conditions, addressing a memory cell generates read currents which clear the cell in preparation for depositing information in the MB, but suppression of the strobe prevents the same amplifiers from producing any output. Any information in the cell is lost.

DCD Set Inputs

Two DCD set inputs are provided. One of these permits a transfer of binary 1's from the corresponding bits of the AC; the other permits a transfer of binary 1's from the data lines of a high-speed I/O device using the data break facility. The AC ⟶ MB and DATA ⟶ MB pulses from MB control trigger the DCD gates.

Jam-Transfer Inputs

Two pairs of DCD gates in each bit permit jam-transfers. One pair is conditioned by the (1) and (0) levels of the corresponding bit of the PC; the other is conditioned by (1) and (0) levels from the next more significant bit of the MB. The gates of bit MB0 are conditioned by complementary MB0 SHIFT ENBL (BS-D-681-0-2, A7, A8) levels; the gates of bits MB1 through MB11 are conditioned by (1) and (0) levels from bits MB0 through MB10, respectively. Thus, the MB acts as a shift register during analog-to-digital conversion operations associated with the Type 189 option or serial character assembly operations associated with the Type 681 option. The jam-transfer from the PC is effected by a PC ⟶ MB command pulse generated in the MB control; the shift operation is effected by an MB SHIFT command pulse generated in the Type 189 Analog-to-Digital Converter (BS-D-189-0-2, C4), or in the Type 681 Data Line Interface (BS-D-681-0-2, B4).

MB Output Signals (16)

The flip-flops of the MB are buffered and drive a 15-ma load at ground from either terminal. Nine Type R650 Bus Driver modules, each containing two drivers, drive the input registers of I/O devices and peripheral equipment. Each driver can drive a 20-ma load at ground or −3v. The MB bus drivers appear on engineering drawing 16 and provide ground assertion levels for bits MB0 (1) through MB11 (1). In addition, ground assertion levels for bits MB3 (0) through MB8 (0) are provided for the device selectors of I/O equipment.

ACCUMULATOR REGISTER AND LINK (2, 16)

The 12-bit accumulator register and the 1-bit link utilize Type R210 double-height flip-flop modules at locations PA6/PB6 (link) and PA7/PB7 through PA18/PB18 (accumulator). Each module contains one

flip-flop, which has a direct clear input, two direct set inputs, a gated complement input, and gated set and reset inputs, together with all the required DCD and NAND gates.

Direct Set and Direct Clear Inputs

All bits of the AC may be simultaneously set to 1 by applying a positive 1 ⟶ AC pulse to the direct set input at terminal AS of each module. Similarly, all bits of the AC may be simultaneously cleared by applying a 0 ⟶ AC pulse to the direct clear input at terminal AR of each module. The link sets or clears independently of the AC by applying 1 ⟶ L or a 0 ⟶ L pulse to link terminal AS or AR, respectively. Each bit of the AC may be set to 1 independently by positive input mixer (IM) pulses at interface connector PE2. Terminals of this interface connector connect to direct-set input terminal AE of each AC module, allowing the AC register to be set by signals from an external device. The direct set input at terminal AE is not used on the link module.

DCD Jam-Transfer Inputs

Four pairs of gates on each module perform rotate operations. One gate in each pair connects to the gated reset input of the flip-flop; the other gate connects to the gated set input. The four pairs of gates are used for RAR, RTR, RAL, and RTL operations. The corresponding command pulses arrive at the appropriate pair of gates in all bits of the AC and in the link simultaneously. The set and reset gates for a given bit, ACn, are conditioned by (1) and (0) levels from another bit of the AC, depending on the operation, as follows:

Operation	Conditioning Source
RAR	ACn-1
RTR	ACn-2
RAL	ACn+1
RTL	ACn+2

DCD Individual Set and Clear Inputs

A DCD clear input is at terminals AK (level) and BR (pulse) of each module. The (0) level of the corresponding MB bit conditions each level input. An MB $\xrightarrow{0}$ AC pulse arrives simultaneously at terminal BR of all modules to logically AND the contents of the AC and the contents of the MB. Terminals AK and BR of the link receive the E SET level from the major state generator and an EAE SETUP pulse during an EAE initializing operation.

DCD set terminals BN and BS permit a transfer of binary1's from the SWITCH REGISTER into the AC. Terminal BS on each module is conditioned or disabled by the corresponding bit of the SWITCH REGISTER.

An SR ⟶ AC pulse arrives at terminal BN of all AC modules simultaneously transferring binary 1's. Terminals BN and BS are not used on the link module. A similar DCD set input at terminals BM (pulse) and BT (level) permits a transfer of binary 1's from bits 0 through 3 of the multiplier-quotient register of the EAE into bits AC0 through AC3. The level input of each AC module is conditioned by the corresponding bit of the MQ; the transfer occurs when an MQ ⟶ AC pulse, originating in the EAE, flows to terminal BM of bits AC0 through AC3 simultaneously. Terminals BM and BT of the link module are not used. Similarly, terminals BM and BT permit an information transfer from the TTI register (keyboard/reader buffer) into bits 4 through 11 of the AC when the Teletype control device selector supplies a TTI ⟶ AC pulse.

Complement Inputs

Complement AC

Each bit of the AC complements individually when a negative COMP ⟶ AC pulse arrives at terminal AM. The pulse inverts and flows to the complementing input of the flip-flop. A separate COMP ⟶ LINK pulse permits the link to complement independently of the AC.

Half Add and Carry

During execution of a TAD instruction, the contents of the MB are added to the contents of the AC in two steps. The first step is a half add (which is simply the inclusive OR for each bit), by a 2-input negative diode NOR gate at the complement input to each AC flip-flop. The second step is a carry performed as a carry initiate, followed by a carry propagate. The transistor gating network shown at the bottom of engineering drawing 2 performs the carry operation. Basically this gating samples the contents of each bit of the AC and MB before the half add takes place, then allows the transients caused by the half add to initiate carry pulses which ripple through the AC towards the link and enable a DCD gate at the next more significant bit, with bit AC0 enabling a gate of the L. When these conditions have settled, the CARRY pulse strobes the DCD gate to set the final result of the addition into the AC with overflow into the link.

A NAND gate in each module has a level input at terminal AK and a pulse input at terminal AN. The output of the gate connects to the complementing input of the flip-flop. The level input of each gate is conditioned by the (1) level of the corresponding bit of the MB; when a HALF ADD pulse arrives at all gates simultaneously, MB bits in the 1 state complement the corresponding bits of the AC.

Transistor gating of the 1 status of each AC bit with the condition of the next less significant bit of the AC enable the DCD gate triggered by the CARRY pulse. The DCD gate associated with a given bit, ACn, becomes enabled when all less significant bits are in the 1 state. The CARRY pulse then triggers the DCD gate and complements these bits, setting them to 0 and setting bit ACn to 1.

During execution of a Group 1 OPR instruction containing a CIA microinstruction, the DCD gate associated with bit AC11 is enabled, and the CARRY pulse complements the flip-flop, incrementing the contents of the AC. Carries are propagated as required.

Analog-to-Digital Conversion

Two DCD gates in each module permit the AC to function as the digital buffer register during an analog-to-digital conversion operation associated with the Type 189 option. The comparator ground level flows to terminal BV, the MBn (1) level to terminal AK, and the MBn+1 (1) level to terminal BU. The A-D CONV pulse from the 189 arrives simultaneously at all the DCD gates at terminal BP.

Accumulator Outputs (16)

The AC produces standard output levels of −3v and ground. The 0 and 1 terminals can each drive a 15-ma external load at ground.

The AC 0 (1) through AC 11 (1) levels are applied to Type R650 Bus Driver modules at locations ME26 through ME28 and MF26 through MF28, in the memory assembly. Each bus driver module contains two drivers. The negative AC (1) levels arrive at the inverting input terminal of each driver; the output levels are ground BAC0 (1) through BAC11 (1) signals. Each bus driver drives a 20-ma external load. The BAC (1) ground levels are made available at interface connectors ME34 and MF34.

SKIP CONTROL (10)

The skip control consists of a skip bus, to which all I/O devices connect, and a pulse amplifier. The skip bus enters the processor at interface connector terminal PF2K and connects to the diode input of pulse amplifier circuit RSVTU in the Type S603 module at location PB21. When the skip bus is driven to ground by circuits in an I/O device, indicating that conditions for an IOT skip instruction are satisfied, the pulse amplifier is triggered and generates a COUNT PC pulse at terminal PB21T. This pulse flows to bit PC11 of the program counter register, incrementing the contents of the PC by 1 and causing the next instruction to be skipped. The COUNT PC pulse produced by an I/O device or the COUNT PC pulse produced by the PC control element increments the contents of the PC.

PROGRAM INTERRUPT SYNCHRONIZATION (10)

When peripheral equipment that is ready to effect an exchange of information with the processor grounds the interrupt bus line, the program interrupt synchronization circuits activate. These circuits, which appear in the lower left portion of engineering drawing 10, determine whether or not the computer can be interrupted to service the peripheral equipment and, if an interrupt enable condition has been established, initiate the program interrupt at the conclusion of the instruction currently being executed. A program interrupt is, in effect, a JMS 0 instruction. The current program count is stored at memory location 0000, and program control transfers to the instruction stored at memory location 0001.

The program interrupt synchronization element consists of a Type S203 Triple Flip-Flop at location PC36 and appropriate gating circuits. These three flip-flops are designated INT. ENABLE (interrupt enable), INT. DELAY (interrupt delay), and INT. ACK (interrupt acknowledge). The INT. ENABLE flip-flop enables or inhibits occurrence of a program interrupt. If this flip-flop is set when a request is made, it enables gates which set the INT. DELAY flip-flop. The INT. DELAY flip-flop enables or inhibits the gates which set the INT. ACK flip-flop delaying the initiation of interrupt operations until completion of the instruction immediately following the ION instruction. When enabled by the INT. ENABLE and INT. DELAY flip-flops and the presence of a ground on the interrupt bus, the INT. ACK flip-flop initiates interrupt operations.

The INT. ENABLE and INT. DELAY flip-flops are cleared by a positive pulse supplied to their direct clear inputs from pulse amplifier output terminal PD33K. This pulse amplifier is triggered by any of the following conditions:

1. By a programmed IOF instruction, DCD gate EF, conditioned by the MB10 (1) level, and triggered by an IOT 00 pulse from the processor device selector at T2A time.

2. By the first T1 pulse occurring after the setting of the INT. ACK flip-flop, DCD gate HJ is conditioned by the ground level at the 1 terminal of the INT. ACK flip-flop and is triggered by the T1E pulse. This action prevents interruption of a granted interrupt.

3. During time state SP1 of a manual start, examine, or deposit operation, NAND gate DEH in module PD36 is conditioned by the negative KEY ST+EX+DP level and is enabled by special timing pulse SP1. The positive pulse appearing at NAND gate output terminal PD36H clears the INT. ACK flip-flop and triggers the pulse amplifier that clears the INT. ENABLE and INT. DELAY flip-flops.

The INT. ACK flip-flop is cleared by manual operations as described in the preceding paragraph. Timing pulse T1E also clears this flip-flop during the execute cycle of the JMS instruction initiated by a program interrupt. However, in this case pull-over action clears the flip-flop, so that the INT. ENABLE and INT. ACK flip-flops are not affected.

Execution of an ION instruction (6001) is the only method of enabling program interrupt operations. DCD gate UV is conditioned by the MB11 (1) level, and during time state T2 the gate is triggered by an IOT 00 pulse from the processor device selector, setting the INT. ENABLE flip-flop to 1.

With the INT. ENABLE flip-flop set, the INT. DELAY flip-flop is set during the next fetch cycle. DCD gate NP in module PC36 is conditioned by NAND combination of the INT. ENABLE (1) and F (1) levels and is triggered by timing pulse T1 of the fetch cycle. This gating assures that one instruction occurs between the last instruction of the interrupt subroutine (the ION) and the next program interrupt.

With the INT. DELAY flip-flop set, the INT. ACK flip-flop can be set as soon as the F SET level appears at the conclusion of an instruction. With an interrupt request signal present on the interrupt bus, DCD gate HJ in module PC36 is conditioned by NAND combination of the INT. DELAY (1) and F SET levels and is triggered by timing pulse T2B. Setting the INT. ACK flip-flop in this manner is inhibited when the INTERRUPT INHIBIT signal is negative. This signal is produced in the Type 183 Memory Extension Control (BS-D-183-0-3, C7) to prevent an interrupt during a change of memory field. The INT. ACK (1) negative level sets flip-flop IR0 to 1, and the INT. ACK (1) ground level disables the input gates of flip-flops IR1 and IR2 so that they cannot be set by signals from the MB. This ground level also conditions a gate in the MA control which causes the MA to be cleared by timing pulse T2B. Thus, whatever instruction is in the MB, the program interrupt forces a JMS 0000 instruction.

The setting of the INT. ACK flip-flop by a combination of F SET, INT. DELAY (1), and T2B signals is inhibited under two conditions:

1. In the absence of a ground level on the interrupt bus, a negative level on the interrupt bus flows to inverter KLN of module PD36. The ground level which appears at terminal PD36N is applied to the node of NAND gate KLMN of module PC35, inhibiting the NAND gate and preventing the INT. ACK flip-flop from being set.

2. In the presence of a negative INT. INHIBIT (1) level, this level flows to inverter PN in module PD31. The ground level appearing at terminal PD31N inhibits the NAND gate in module PC35, as described in 1. The INT INHIBIT level generates in the memory extension control and prevents an interrupt from occurring between execution of a CIF instruction and execution of the JMS or JMP instruction that changes the instruction field.

TYPE KR01 AUTOMATIC RESTART OPTION

This option protects an operating program in the event of failure of the source of computer primary power. If a power failure occurs, this option causes a program interrupt and forces the PWR OK level for 1 msec, allowing the interrupt routine to detect the power low condition as initiator of the interrupt, and to store the contents at active registers (AC, L, MQ, etc.) and the program count in known core memory locations. When power is restored, the power low flag clears and a routine beginning in address 0 automatically starts. This routine restores the program count and active registers to the conditions that existed when the interrupt occurred, then continues the interrupted program.

The KR01 option consists of five modules in locations PF5 through PF9, and circuits from existing modules in locations PE12 and PE14. The logic circuits of this option appear on engineering drawing BS-D-KR01-0-2. Interface between the basic PDP-8 processor and the KR01 option is indicated in Table 3-1.

TABLE 3-1 AUTOMATIC RESTART OPTION INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction	KR01 Option Terminal
	Logic Element	Engineering Drawing	Terminal		
PWR STATUS	Timing	9	PB30H	——◇	PF5M
PWR OK	Timing	9	PB30F	◆——	PF5F
INT BUS IN	Interrupt Sync	10	PF2M	◇——	PF5D
COUNT PC ENABLE	PC Control	10	PF1R	◁——	PF5T
PC CLEAR	PC Control	8	PD22L	◁——	Switch (PF7E)
KEY START	Manual Control	9	PA5P	◇——	PF5N
IOP2	IOP Generator	10	PF1KK	——▷	PF5S
MB3 (0)	MB	5	PD1R	——◆	PF6H
MB4 (0)	MB	5	PD1T	——◆	PF6J
MB5 (1)	MB	5	PE1E	——◆	PF6L
MB6 (0)	MB	5	PE1F	——◆	PF6M
MB7 (0)	MB	5	PE1J	——◆	PF6P
MB8 (0)	MB	5	PE1L	——◆	PF6R

Logic circuits of the automatic restart option consist of a power failure detection and interrupt request element, a circuit to add an instruction to the computer repertoire to skip on the power low condition, and an automatic restart element.

The POW STATUS output of the Type 708 Power Supply is the input to the KR01. This level is at −3v when power is on and is at ground when power is interrupted (due to a power failure or due to operation of the POWER lock on the operator console). When power fails, the positive transition of this level is sensed by a Schmitt trigger that produces an output that goes to ground level. This latter positive transition sets a PWR LOW flip-flop and initiates a 1-msec delay. The buffered output of the delay holds the POW OK level at −3v for approximately 1 msec after power fails, preventing generation of PWR CLR pulses during this interval. A 0.01 μf capacitor from this signal line to ground holds the line negative during the transition between power failure and the negative output of the buffer inverter.

When the PWR LOW flip-flop is set, the buffered PWR LOW flag signal (INT BUS IN) requests a program interrupt. The interrupt routine has 1 msec to sense the condition of this flag and execute a subroutine that stores the program count and the contents of the active registers. For a basic PDP-8 with an extended arithmetic element, this subroutine can be performed in 25.5 μsec.

Since the time that operation of the computer can be extended after a power failure is limited, the condition of the PWR LOW flag should be the first status check made by the interrupt routine. Sensing of this flag is accomplished by a skip on power low (SPL = 6102) instruction. An 8-input NAND gate for negative levels composed of the Type R002 Diode Network module at location PF6 and inverter VT of the S107 model at location PF5 executes this instruction. Inputs to this gate are conditioned when the PWR LOW flag is a 1, and the SPL instruction is executed. The positive pulse output of this gate connects to the COUNT PC ENABLE line of the processor to generating a COUNT PC pulse and incrementing the program count by one to skip over the next sequential instruction.

When power is restored the Schmitt trigger output returns to a −3v level. The buffered leading edge of this level triggers DCD gate ST of the Type S602 Pulse Amplifier module at location PF9 at the end of the 1-msec delay. If power is restored within 1 msec, the positive transition of the output of the delay triggers DCD gate PR of this module at the end of the delay time. This gating network makes the KR01 insensitive to power transients that occur more frequently than 1 msec apart (e.g., caused by contactor chatter), preventing numerous program interrupts during periods of unstable primary power. Either of these gates triggers the pulse amplifier to clear the PWR LOW flip-flop, and, if the RESTART switch on the processor marginal-check frame is in the down, or ON, position, restarts the program.

With the RESTART switch closed, the positive pulse output at terminal PF9U triggers pulse amplifiers in the PC control element to produce pulses that clear the entire PC. This pulse output also triggers a two-delay time chain to produce a KEY START level. This KEY START level restarts programmed operation of the computer. Since the PC contains 0000, the program begins by executing a subroutine that restores the conditions that existed when the power failure occurred, then resumes the interrupted program.

The first delay in the time chain causes a delay of 160 msec between power restoration and program restart. This time delay allows slow mechanical devices, such as Teletype equipment, to come to a complete mechanical stop before continuing the program. The second delay in the time chain triggers at expiration of the 160-msec delay. The output of this second delay forces a buffered KEY START level for the 40-msec delay time. This signal simulates pressing the START key on the operator console and initiates operation of the special pulse generator in the processor. The long duration of this level is required to pass through the integrator of the Schmitt trigger at the input of the SP generator.

TYPE 182 EXTENDED ARITHMETIC ELEMENT

The extended arithmetic element is a standard option for the PDP-8 which enables the processor to perform arithmetic operations at higher speeds. Higher speeds are made possible by incorporating the EAE components with the existing processor logic. These components are a 12-bit multiplier quotient register (MQ), a 5-bit step counter (SC), a 3-bit instruction register (EAE IR), and EAE timing and control logic.

The EAE logic is installed in positions 17 through 36 of rows PE and PF of the processor module mounting assembly. The content of the MQ register is displayed on the MULTIPLIER QUOTIENT indicators located below the operator console ACCUMULATOR indicators. The EAE logic block diagrams are engineering drawings BS-D-182-0-2 and BS-D-182-0-3. The EAE flow diagram is engineering drawing BS-D-182-0-4.

Logical Functions

The circuits of the EAE are used in conjunction with the link, AC, and MB in the processor to perform parallel arithmetic operations on positive binary numbers. Figure 3-1 is a simplified block diagram of the EAE option.

The EAE uses a class of Group 2 OPR instructions containing binary 1's in bits 3 and 11. Refer to Figure 1-3(e) for the EAE instruction format and to the PDP-8 Users Handbook for a description of the EAE instructions. Information transfers between registers of the EAE and the processor occur during the fetch cycle of EAE instructions. Arithmetic operations require as much as 36 μsec to complete; therefore, an EAE instruction microprogrammed for arithmetic operations sets the PAUSE flip-flop in the processor to prevent advancement of the computer program. When arithmetic operations end, the EAE produces a RESTART SYNC signal which causes the processor to resume the program. Arithmetic operations other than normalizing require an execute cycle as well as a fetch cycle, and the logic elements of the EAE generate an E SET signal which causes the processor to enter the execute state.

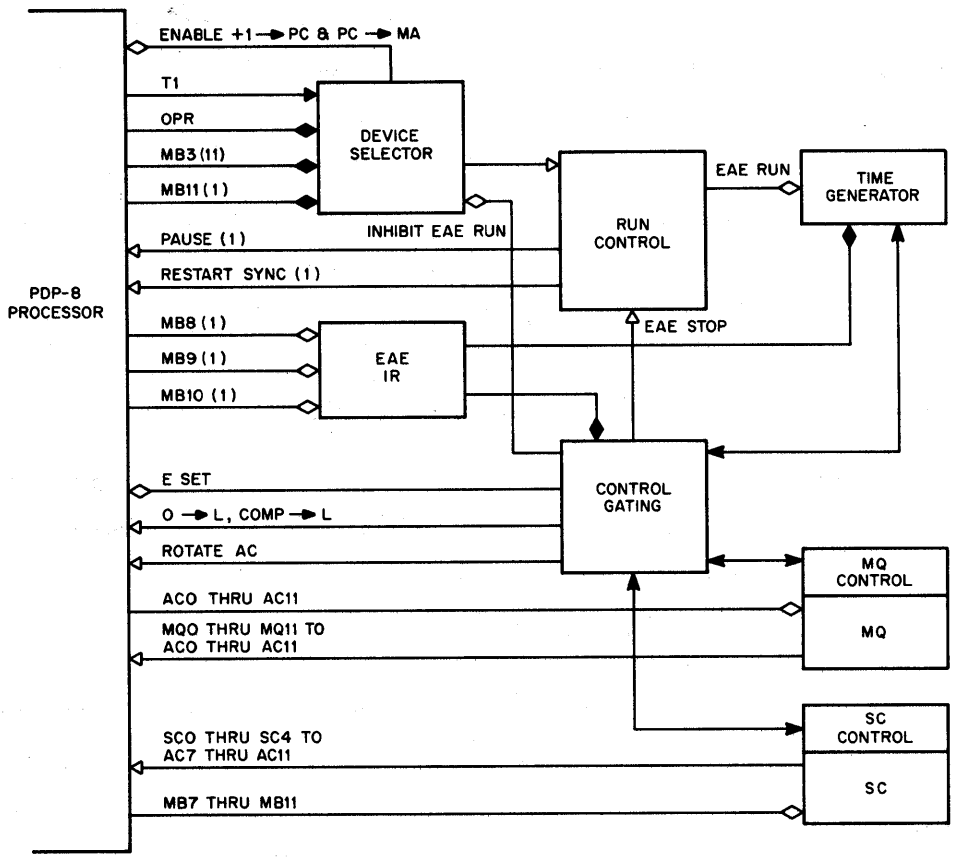


Figure 3-1 Type 182 Extended Arithmetic Element Simplified Block Diagram

Single-Cycle Operations

Four operations are microprogrammed by bits 4 through 7 of the instruction word and are completed during the fetch cycle. These instructions are CLA, MQA, SCA, and MQL. One arithmetic operation, NMI (normalize), requires a pause during which the EAE time generator runs, but is also completed during the fetch cycle.

Reference to the flow diagram shows that during time state T1 in the fetch cycle of the EAE instruction, the SC and the EAE IR are automatically cleared. If CLA (clear AC) is microprogrammed by a 1 in bit 4, the AC clears. If NMI is microprogrammed by a 1 in bit 8, the EAE run control starts the EAE time generator and stops the processor timing. During the normalizing operation, the combined contents of the MQ and AC repeatedly shift left until the contents of bit AC0 are not equal to the contents of bit AC1, or until the combined AC and MQ contains 6000 0000. At each shift, 0's are inserted into vacated low-order MQ bits. At the conclusion of this operation, the original binary number has been transformed into an exponent which corresponds to the number of shifts performed and is held in the SC, and a fraction held in the AC and MQ. The exponent and the fraction may be loaded (separately) into the AC and deposited in memory.

Further operations may be microprogrammed during time state T2. If MQA is microprogrammed by a 1 in bit 5 of the EAE instruction, the contents of the MQ are loaded into the AC. Note that this operation does not automatically clear the AC; if the contents of the AC are not 0 before the EAE instruction, the AC must be cleared either by a DCA instruction or by combining a CLA microinstruction with the MQA. If SCA is microprogrammed by a 1 in bit 6, the contents of the step counter transfer into the AC. Again, the AC should be cleared prior to giving this instruction, or a CLA command should be combined with the SCA. If MQL is microprogrammed by a 1 in bit 7, the MQ clears, then the contents of the AC transfers into the MQ and the AC automatically clears.

The absence of 1's in bits MB9 and MB10 indicate that no further arithmetic operation is to be performed. The MB clears, the contents of the PC are set into the MA, and the processor enters the fetch cycle of the next instruction. However, if either bit 9 or 10 contains a 1, the major state is set to execute in preparation for the execution of an arithmetic operation requiring an additional reference to memory.

Two-Cycle Instructions

There are five 2-cycle EAE instructions which are selected by the octal operation code in bits 8 through 10 of the instruction word. This operation code transfers into the EAE IR during time state T2 of the fetch cycle, and the operation is performed during the execute cycle. An EAE instruction may be microprogrammed to perform one 2-cycle instruction and one or more 1-cycle operations that are logically compatible with the 2-cycle instruction. For example, MQL is an essential preparation for a multiply or divide operation, and the MQL and MUY commands can be combined in the same EAE instruction.

Multiply (MUY) - The MUY command has a 1 in bit 9 of the EAE instruction, corresponding to an EAE operation code 2_8. During the fetch cycle, an MQL microinstruction loads the multiplier into the MQ and then clears the AC and link. During the execute cycle, the multiplicand is retrieved from memory and held in the MB. The PC increments in time state T1; then, in time state T2, the EAE run control produces a pause state in the processor and starts the multiplication. When multiplication is completed, the twelve most significant bits of the product are in the AC, and the twelve least significant bits of the product are in the MQ. The EAE time generator stops, the processor time generator restarts, the contents of the PC are set into the MA, the MB clears , and the processor enters the fetch cycle of the next instruction.

The algorithm for multiplication is simply shift right and add. Multiplication operations begin with the multiplicand in the MB, the multiplier in the MQ, and a cleared AC and link. The least significant bit of the multiplier is sampled, and if it contains a 1, the multiplicand is added to the partial product in the AC. If the least significant bit of the multiplier contains a 0, the addition is not performed since any number

multiplied by 0 equals 0. Then the contents of the AC and the MQ shift together one position to the right; therefore, one bit of the product shifts into the MQ, and the bit of the multiplier just used is lost. The following example illustrates this operation performed on 4-bit numbers for the problem: 15 x 5.

	MB 1111		Start with multiplicand in MB, multiplier in MQ, and with AC and link cleared.
L0	AC 0000	MQ 0101	
	1111		Since MQ11=1, add. After the addition shift L, A, MQ right one position.
0	0000	0101	
0	1111	0101	
	1111		After the shift MQ11=0; therefore do not add, just shift.
0	0111	1010	
	1111		After the shift MQ11=1; add, then shift.
0	0011	1101	
1	0010	1101	
	1111		After the shift MQ11=0; do not add, just shift
0	1001	0110	
	1111		After the shift the most significant half of the product is in the AC, and the least significant half of the product is in the MQ.
0	0100	1011	

This operation is analogous to solving the problem by hand as follows:

```
  1 1 1 1        multiplicand in MB
x 0 1 0 1        multiplier in MQ
---------
  1 1 1 1
0 0 0 0
1 1 1 1
0 0 0 0
---------
0 1 0 0 | 1 0 1 1 = 75
  AC    |   MQ
```

Divide (DVI) - The DVI command has 1's in bits 9 and 10 of the EAE instruction, corresponding to the EAE operation code 3_8. The DVI command must be preceded by loading instructions as follows:

1. A TAD instruction loads the twelve least significant bits of the dividend into the AC.
2. An EAE instruction containing an LMQ command loads the contents of the AC into the MQ.
3. A second TAD instruction loads the twelve most significant bits of the dividend into the AC.

During the fetch cycle of the EAE instruction containing the DVI command, the contents of the PC are set into the MA; the DVI command is set into the EAE IR; and the MB clears. During the execute cycle, the divisor is retrieved from memory and held in the MB. During time state T1, the contents of the PC increment by 1 and the contents of the AC are complemented to invert the dividend. During time state T2, the EAE run control produces a pause state in the processor timing and starts the division. When the division is completed, the quotient is in the MQ, the remainder in the AC, and a 0 in the link. The EAE time generator stops, the processor time generator restarts, the contents of the PC are set into the MA, the MB clears, and the processor enters the fetch state of the next instruction.

The algorithm for division is subtract and rotate left. Division begins with the divisor in the MB, the most significant half of the dividend in the AC, and the least significant half of the dividend in the MQ. The most significant portion of the dividend is subtracted from the divisor. If the result is a positive number, a 1 is placed in the quotient; if the result is a negative number, a 0 is placed in the quotient. If the result of the first subtraction is a positive number, divide overflow occurs to stop the operation and to allow rescaling of either argument. If the result of the subtraction is a positive number in any cycle but the first one, the dividend rotates left one binary place with respect to the divisor, and the operation continues with another subtraction. In some binary division hardware, a subtraction which results in a negative number is followed by an addition to restore the dividend; the dividend rotates left one binary place, and subtraction repeats to determine the next bit of the quotient. If the divisor is represented by A and the dividend is represented by B, each cycle of this operation is $A - B + B - 1/2B = A - 1/2B$. To simplify this operation the Type 182 option subtracts, does not add the divisor to the result of the subtraction, then adds one half of the dividend to the quotient. Each cycle of this operation can be represented as $A - B + 1/2B = A - 1/2B$. The following example illustrates this operation in a problem containing an 8-bit dividend and a 4-bit divisor, quotient, and remainder.

Problem: $85 \div 9$ or $0101\ 0101 \div 1001$

	1001		Begin with divisor in MB, least significant half of the dividend in MQ, the complement of most significant half of the dividend in AC, and a 1 in L.
1	1010	0101	
	1001		First cycle, so add divisor to most significant half of dividend.
1	1010	0101	
0	0011	0101	
	1001		First cycle, so complement the contents of AC and L.
1	1100	0101	

	1001		Rotate the contents of the L, AC, and MQ left so that the complement of the content of the L is set into the least significant bit of the MQ, which is MQ11.
1	1000	1010	
	1001		MQ11 = 0 so do not complement, just add.
1	1000	1010	
0	0001	1010	
	1001		Rotate left as before.
0	0011	0101	
	1001		MQ11 = 1 so complement the contents of the AC and L, add the contents of the MB to the contents of the AC, and recomplement the contents of the L and AC.
1	1100	0101	
0	0101	0101	
1	1010	0101	
	1001		Rotate left as before.
1	0100	1010	
	1001		MQ11 = 0 so do not complement, just add.
1	0100	1010	
1	1101	1010	
	1001		Rotate left as before.
1	1011	0100	
	1001		Since MQ11 = 0, do not complement, just add.
1	1011	0100	
0	0100	0100	
	1001		Last cycle so rotate L and MQ, but do not rotate AC; L = 0 so halt. Quotient is now in MQ and remainder is in AC.
0	0100	1001	

If the L = 1 after performing a number of cycles equal to the number of bits in the divisor +1, another half cycle of operation is performed to produce an accurate remainder by adding the divisor to the contents of the AC.

Shift Arithmetic Left (SHL) - The SHL command is identified by binary 1's in bits 8 and 10 of the EAE instruction, corresponding to an EAE operation code 5_8. During the fetch cycle of an SHL command, the EAE operation code is set into the EAE IR and the MB clears. During the execute cycle a binary

number is retrieved from core memory and set into the MB. This number represents the number of left shifts to be performed, less 1. During time state T1 the contents of the PC increment by 1. During time state T2 the number held in the MB transfers into the SC. The EAE run control produces a pause state in the processor and starts the shifting operation. When this operation is completed, the EAE stops, the processor time generator restarts, and the processor enters the fetch cycle of the next instruction. During the shift operation, the L, AC, and MQ are treated as one long register.

Arithmetic Shift Right (ASR) - The ASR command is identified by binary 1's in bits 8 and 9 of the EAE instruction, corresponding to an EAE operation code 6_8. The sequence of events during this instruction is similar to that which takes place during the SHL instruction, except that the shift is to the right. The sign bit in AC0 is preserved during the shift by setting the link to correspond with the contents of AC0. Information shifted out of MQ11 is lost.

Logical Shift Right (LSR) - The LSR command has binary 1's in bits 8, 9, and 10 of the EAE instruction, corresponding to an EAE operation code 7_8. The sequence of events during this instruction is similar to that which takes place during the ASR instruction, except that AC0 and the link clear during the first shift. The sign is therefore lost, and 0's enter all vacated positions.

Functional Components

Device Selector (182-0-3)

The EAE is selected as a function of an OPR instruction containing binary 1's in bits 3 and 11. The OPR, F(1), MB3(1), and MB11(1) levels combine in NAND gate RSTU of module PE35 (zone D2). Negative and ground EAE INST levels appear at terminals PE30R and PE35U, respectively. These levels are used for clearing the flip-flops of the timing signal generator, instruction register, and step counter, and for gating control signals within the EAE.

EAE Run Control (182-0-3)

The EAE run control consists of the EAE ON flip-flop and the EAE RUN flip-flop, both contained in a Type S203 Triple Flip-Flop module at location PE32. The EAE ON (1) level controls the timing cycle of the EAE and performs other gating in the control circuits. The EAE RUN (1) level enables the timing signal generator. The EAE RUN flip-flop is set by a DCD gate in its set-to-1 input. The gate, conditioned by a ground EAE ON (1) level, is triggered by the next EAE CLOCK pulse. The EAE RUN flip-flop is cleared by the ground level arriving at its direct clear input. This level generates when the EAE ON flip flop is cleared by an EAE STOP pulse arriving at its direct clear input.

The EAE ON flip-flop is set by one of the following conditions:

1. During the execute cycle of an EAE instruction, DCD gate JH of module PE32 (zone C1) is conditioned by an OPR level from the processor major state generator and is triggered by timing pulse T2E. This timing pulse generates only during an execute cycle; therefore, the flip-flop is not set by any processor OPR instruction, since such instructions are all completed during a fetch cycle.

2. During the fetch cycle of an instruction which is microprogrammed to normalize a binary number to a fraction and an exponent, NAND gate RSTU of module PE34 is conditioned by negative EAE INST, $\overline{\text{E SET}}$, and MB8 (1) levels and is triggered by timing pulse T1. The positive pulse appearing at terminal PE34U sets the EAE ON flip-flop to 1 by pull-over action and triggers pulse amplifier TUV in module PE31 to produce a PAUSE (1) pulse. However, conditioning of the NAND gate may be overridden by a ground potential applied to the node terminal, PE34T. When a ground is applied, the gate is inhibited and does not set the EAE ON flip-flop or generate a PAUSE (1) pulse. Inhibiting occurs when the contents of bit AC0 differ from those of bit AC1, as indicated by a ground output from NAND gate DEH or from NAND gate KLN in module PE36 or when a ground NORMALIZED level is applied to the node of NAND gate RSTU in module PE34 by the gates which sample the contents of the AC and of bit MQ11 (182-0-2).

The EAE STOP pulse which clears the flip-flops of the EAE run control generates from pulse amplifier VUN in module PF30 (zone C8). This pulse amplifier may be triggered by an MQ SHIFT LEFT pulse, an MQ SHIFT RIGHT pulse, and EAE CARRY pulse, or by an SC = 0 pulse.

The EAE STOP pulse generates from an MQ SHIFT LEFT pulse when a ground level conditions DCD gate ST in module PF30 (zone C8). This ground level is produced by any of the following conditions:

1. Bit AC1 contains a 1, bit AC2 contains a 0, and EAE IR2 contains a 0 indicating that the number will be normalized at this shift pulse.

2. The link contains a 0, EAE IR0 contains a 0, and SC1 and SC2 each contain a 1 indicating that a normalize instruction is being executed.

3. Bit AC1 and EAE IR2 each contain a 0, bit AC2 contains a 1 which also indicates that the number will be normalized at this shift pulse.

The EAE STOP pulse is generated by an MQ SHIFT RIGHT pulse when DCD gate PR in module PF30 is conditioned by a ground level. This ground level is produced when EAE IR2 contains a 0 (MUY instruction) and SC1, SC3, and SC4 each contain a 1 (SC = 12).

The EAE STOP pulse generates from a positive-going level transition as flip-flop SC0 changes from the 1 to the 0 state indicating that the required number of shifts have been completed. DCD gate EF in module PF30 is permanently conditioned by a ground level and is triggered by the SC0 (0) transition. The output pulse from the gate triggers pulse amplifier LK in module PF30, which in turn triggers pulse amplifier VUN to produce the EAE STOP pulse

The EAE STOP pulse generates from a positive EAE CARRY pulse when DCD gate HJ in module PF30 is conditioned by a ground level. The ground level is produced when EAE IR2, (DVI instruction), SC1, SC2, and SC4 each contain a 1 (SC = 14) indicating that restoration of the remainder is complete.

The EAE STOP pulse generates from a negative pulse appearing at the output of NAND gate RSTU in module PE36 (zone C5). The gate is conditioned by SC = 0, $\overline{\text{LINK CARRY}}$, and EAE IR2 (1) levels, and is enabled by the negative EAE CARRY pulse indicating that divide overflow conditions exist during the first divide operation of a DVI instruction.

EAE Time Generator

The EAE time generator consists of three flip-flops, designated ATG0, ATG1, and ATG2, and a Type R405 Crystal Clock. These components appear in the upper portion of engineering drawing BS-D-182-0-3. The flip-flops act as a binary frequency divider, and their (1) and (0) levels are decoded to produce five sequential gating conditions in the logic that controls addition and subtraction steps during arithmetical operations. Additions require only the first three of these conditions; subtraction, which involves both complmentation and addition, requires all five conditions.

The EAE RUN (1) level permits the crystal clock to trigger pulse amplifier FH in module PE31 at each clock pulse. The output of the pulse amplifier then complements flip-flop ATG2 at each clock pulse. Gating at the input of the ATG flip-flops causes flip-flop ATG1 to set at the second pulse and to clear at the third during an addition step, and flip-flop ATG0 to set at the fourth clock pulse and to clear at the fifth during a subtraction step. (See timing diagram in zone A1 of drawing BS-D-182-0-3.) During initializing operations the processor T1 pulse arrives at the direct clear input of flip-flop ATG2 and clears flip-flops ARG0 and ATG1 by pull-over action.

EAE Instruction Register (182-0-3)

The EAE IR is a 3-bit register consisting of a Type S203 Triple Flip-Flop in module PE33 (zones C3, C4). All three flip-flops are cleared by applying the processor 0 ⟶ IR pulse to their direct set inputs.

DCD gates in the set-to-1 inputs of flip-flops EAE IR0 through EAE IR2 are conditioned by ground levels from bits MB8 through MB10, respectively. When an EAE SETUP pulse arrives at all three gates simultaneously, binary 1's from the MB bits are set into the EAE IR. The EAE SETUP pulse generates from pulse amplifier TU in module PE29 (zone A8). The DCD input gate of this pulse amplifier is conditioned by the EAE INST level from the device selector and is triggered by timing pulse T2A from the processor.

The (1) and (0) levels of the EAE IR flip-flops are used in the control logic for gating.

E SET Signal (182-0-3)

The E SET generator consists of NAND gates DEH and KLN in module PE34 (zone B3). The ground level E SET signal generates during any EAE instruction containing a 1 in bit 9 or 10 (i.e., MUY, DVI, SHL, ASR, or LSR). All 2-cycle EAE instructions contain a 1 in either bit MB9 or MB10. The MB9 (1) or MB (1) level combines with the EAE INST level and causes the associated NAND gate to produce a ground E SET level which forces the processor major state generator to establish an execute state during the following cycle.

Register Control Logic

The register control logic consists of all the gates and pulse amplifiers required to transfer information between registers of the EAE and processor and to clear or complement these registers. The following paragraphs describe each signal produced by the control logic.

EAE SETUP Signal (182-0-3) - The EAE SETUP signal generates from pulse amplifier TU in module PE29 (zone A8). DCD gate RS associated with this pulse amplifier is conditioned by a ground EAE INST level whenever an EAE instruction is executed and is triggered by timing pulse T2A from the processor. The EAE SETUP pulse transfers binary 1's from bits MB8 through MB10 into the EAE IR and also triggers generation of other control signals as a function of the contents of bits MB4 through MB7.

MQ ⟶ AC Signal (182-0-2) - This signal generates from pulse amplifier FH in module PE23. The DCD input gate of this pulse amplifier is conditioned by a ground MB5 (1) level (identifying an MQA microinstruction) and is triggered by the EAE SETUP pulse at processor time T2A. The pulse amplifier positive output flows to inverter DE in module PE22 to obtain complementary MQ ⟶ AC pulses. The contents of bits MQ4 through MQ11 are set into the corresponding bits of the AC by this pulse.

SC ⟶ AC Signal (182-0-2) - This signal generates from pulse amplifier MN in module PE23. The DCD input gate of this pulse amplifier is conditioned by an MB6 (1) ground level (indicating an SCA microinstruction) and is triggered by the EAE SETUP pulse. The positive output of the pulse amplifier is applied to inverter FH in module PE22. A negative SC ⟶ AC pulse appears at inverter output terminal

PE22F, and this pulse transfers the contents of the SC into bits AC7 through AC11. The gates which perform the transfer appear in the top right portion of engineering drawing BS-D-182-0-2.

AC ⟶ MQ Signal (182-0-2) - This signal generates from pulse amplifier TU in module PE23. The DCD input gate of this pulse amplifier is conditioned by an MB7 (1) level (indicating an MQL microinstruction) and is triggered by the EAE SETUP pulse. The positive AC ⟶ MQ signal appears at pulse amplifier output terminal PE23T and opens DCD set-to-1 gates of the MQ flip-flops. These gates are conditioned by the AC (1) levels and triggered by the AC ⟶ MQ pulse.

0 ⟶ MQ Signal (182-0-2) - This positive pulse is generated by NAND gate DEFH in module PF24 (zone D1). The gate is conditioned by EAE INST and MB7 (1) levels and is enabled by timing pulse T1 from the processor. The 0 ⟶ MQ pulse generates during time state T1 of an EAE instruction containing an MQL microinstruction, and clears the MQ in preparation for the transfer of binary 1's from the AC which takes place in time state T2.

MB7-11 ⟶ SC Signal (182-0-2) - This positive pulse generates from pulse amplifier FH in module PF28. The DCD input gate of this pulse amplifier is conditioned by a ground level produced by NAND combining the OPR and EAE IR0 (1) levels and is triggered by timing pulse T2E during the execute cycle of any EAE instruction microprogrammed for a shift operation.

EAE SHIFT Signal (182-0-3) - This positive pulse generates at pulse amplifier output terminal PE31T at each T3 time of an EAE short cycle or at each T4 time of an EAE long cycle. The pulse amplifier triggers each time the ATG1 flip-flop changes from the 1 to the 0 state when the input DCD gate is conditioned by the EAE ON (1) level. This pulse triggers gated pulse amplifiers that produce specific shift pulses.

MQ SHIFT LEFT Signal (182-0-3) - This positive signal is produced by pulse amplifier UN in module PF23. During divide operations, DCD input gate ST is conditioned by the EAE IR2 (1) level and is triggered by the EAE SHIFT pulse each time flip-flop ATG1 changes from the 1 state to the 0 state. During normalizing and shifting operations, DCD gate PR is conditioned by NAND combining the EAE IR0 (1) and EAE IR1 (0) levels and is triggered at every EAE clock pulse.

MQ SHIFT RIGHT Signal (182-0-3) - This positive pulse generates from pulse amplifier EFK in module PF23. During multiply operations, DCD input gate HJ is conditioned by the EAE IR2 (0) levels and is triggered by the EAE SHIFT pulse each time flip-flop ATG1 changes from the 1 state to the 0 state. During arithmetic and logical shift operations, DCD gate EF is conditioned by NAND combining the EAE IR0 (1) and EAE IR1 (1) levels and is triggered at each EAE clock pulse. During a multiply operation, DCD gate EF is conditioned by NAND combining the MQ11 (0), EAE IR2 (0), and EAE IR1 (1) levels and is triggered at each EAE clock pulse.

EAE AC ROTATE LEFT Signal (182-0-3) - This positive pulse generates from pulse amplifier MN in module PE31. DCD input gate KL is conditioned by the DIV LAST ground level and triggers on the MQ SHIFT LEFT pulse. The EAE AC SHIFT LEFT pulse shifts the contents of the AC each time the contents of the MQ are shifted left until the step counter is full, indicating the last EAE cycle is occurring.

DIV LAST Signal (182-0-3) - This negative level occurs during a divide operation when the step counter reaches a count of 12, indicating that the last cycle is in progress unless the remainder must be restored. This signal generates in a 4-input diode gate composed of gate KLN of the module at PF31 and gate DEF of the module at PF33. Until the last cycle is reached the DIV LAST signal is at ground and enables the pulse amplifier producing the EAE AC ROTATE LEFT pulse. In the last cycle this pulse amplifier is inhibited and the gating circuits that produce the EAE STOP pulse are enabled by the negative DIV LAST level.

EAE HALF ADD Signal (182-0-3) - This positive pulse generates during multiply and divide operations by pulse amplifier FH in module PE29. DCD input gate DE is conditioned by the ATG1 (0) level and is triggered by the transition of the ATG2 flip-flop from the 0 to the 1 state. The EAE HALF ADD pulse appears at terminal PE29F and is applied to the AC control. When this pulse generates, it causes the contents of the MB to be half-added to the contents of the AC. An EAE CARRY pulse completes the addition.

EAE CARRY Signal (182-0-3) - This pulse generates from pulse amplifier MN in module PE29. DCD gate KL is conditioned by a ground and is triggered by the transition of the ATG1 flip-flop from the 0 to the 1 state. The positive EAE CARRY pulse appears at pulse amplifier output terminal PE29M; the negative EAE CARRY pulse appears at inverter output terminal PE30D. The pulse flows to the AC control, where it causes generation of an AC CARRY pulse to propagate carries in the AC during addition.

EAE LINK COMP and EAE AC COMP Signals (182-0-3) - Pulse amplifier LK in module PC30 generates the EAE AC COMP positive pulse that is inverted to produce the EAE LINK COMP positive pulse. The positive output pulse appears at terminal PC30K, and the negative pulse at inverter output terminal PE30T. They are both generated by one of the following conditions:

1. DEC gate HJ is conditioned by the EAE ON (1) level and is triggered when flip-flop ATG0 changes from the 1 state to the 0 state during a subtract step.

2. DCD gate EF is conditioned by the ATG1 (1) level and is triggered when the ATG2 flip-flop changes from the 0 to the 1 state.

3. During a divide operation, NAND gate RSTU in module PF34 is conditioned by OPR, EAE IR0 (0) and EAE IR2 (1) levels and is enabled by timing pulse T2E from the processor. The positive pulse appearing at terminal PF34U triggers the pulse amplifier that produces the complementing pulses.

0 ⟶ LINK Signal (182-0-3) - This pulse is produced during a MUY or ASR operation. NAND gate DEFH of module PF34 is conditioned by EAE ON (1), EAE IR1 (1), and EAE IR0 (1) levels and is enabled when clearing of the AC causes bit AC0 to change to the 0 state. The pulse appears at terminal PF34H.

1 ⟶ LINK Signal (182-0-3) - This pulse sets the link to 1 during an ASR operation. If bit AC0 is in the 1 state, the AC0 (1) level conditions one input of NAND gate KLMN in module PF34. The other inputs are conditioned by EAE ON (1), EAE IR0 (1), EAE IR1 (1), and EAE IR2 (0) levels. These levels cause the gate to produce a positive level at terminal PF34H. The level flows to the processor, where it sets the link to 1, preserving the original sign of the number in the AC and MQ.

MQ Register (182-0-2)

The multiplier-quotient register consists of six Type R212 FLIP CHIP Dual Flip-Flop modules specifically designed for assembly into a bidirectional shift register. These six modules are in positions PF17 through PF22 and contain five DCD input gates per flip-flop. One pair of these is used for shift right operations, one pair is used for shift left operations, and the fifth gate transfers binary 1's from the AC into the corresponding bits of the MQ. Each flip-flop drives an external load of 9 ma at ground from the 0 terminal, and 11 ma at ground from the 1 terminal. If either the link contains a 1, or EAE IR0 contains a 1, a shift left operation sets bit MQ11 to 0. If both the link and EAE IR0 contain 0's a shift left operation sets bit MQ11 to 1.

Step Counter (182-0-2)

The step counter (SC) is a 5-bit register composed of Type S205 Dual Flip-Flop modules. During shift operations, the number equal to one less than the number of shifts to be performed (in binary form) is set into the SC from bits MB7 through MB11. This number is stored at the core memory location consecutively following the location which contains the EAE instruction. The SC counts the number of shifts performed and halts the shifting process when bits SC1 through SC4 all contain 0's.

During multiply and divide operations, the SC counts the steps performed and halts the operation when the appropriate number of steps have been completed.

TYPE 681 DATA LINE INTERFACE OPTION

The 681 is a prewired option of the PDP-8 that enables use of the computer with a Type 680 Data Communications System. Basically, the 681 adds two instructions to the computer to simplify input and output transfers of Teletype information. The fundamental principles of the 680 system must be known to understand the function of the 681.

Type 680 Data Communication System Block Diagram Discussion

The 680 Data Communication System allows up to 128 local or distant Teletype units to communicate with the computer. A 680 system configuration varies according to the number, type, and distribution of the Teletype units it contains, and upon the use to be made of the system. System configuration appears in Figure 3-2.

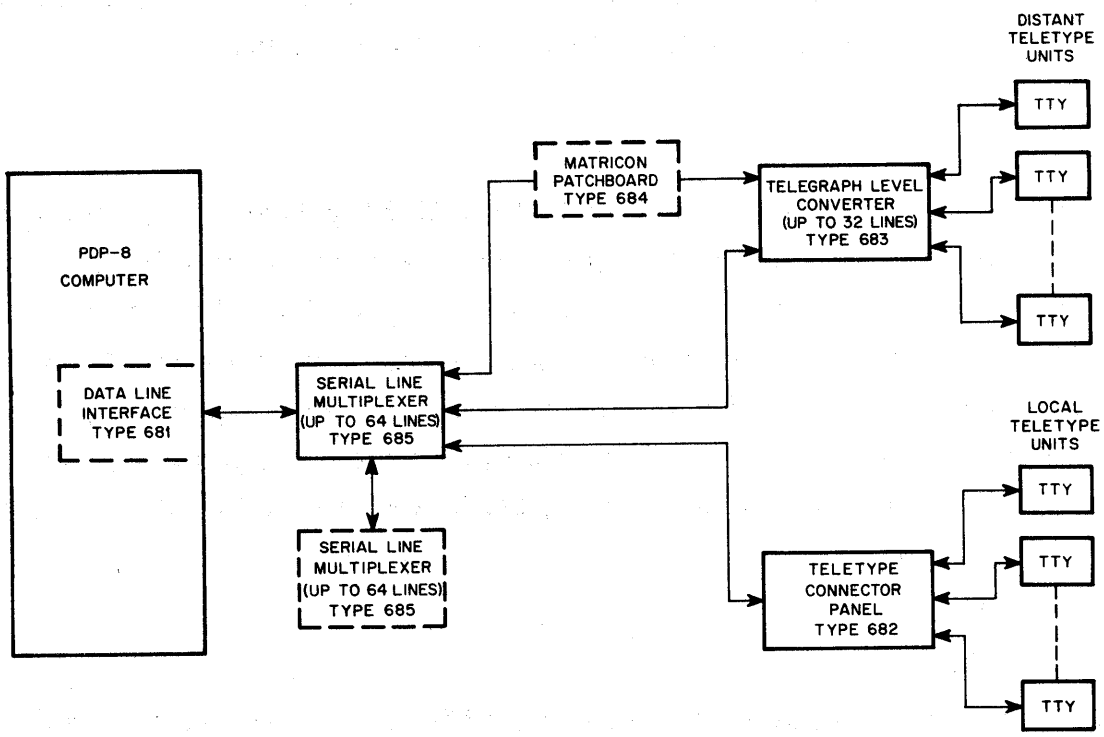


Figure 3-2 Type 680 Data Communications System Block Diagram

Teletype connections from remote stations are received and transmitted by a Type 683 Telegraph Level Converter. Teletype connections for local units are made by a Type 682 Teletype Connector Panel. Teletype signals for each station run from the 682 or 683 to a Type 685 Serial Line Multiplexer. A Type 684 Matricon Patchboard also provides manual selection of channel connections between the 683 and the 685. The 685 consists of a multiplexer for Teletype lines and a clock that causes a program

interrupt at a rate eight times the line baud frequency. Single line connections are made between the 685 and the Type 681 Data Line Interface and between the 685 and the normal interface of the computer. The 681 provides an output instruction to transfer Teletype information from the accumulator to the 685, and provides an input instruction to read Teletype information directly into the computer core memory from the 685. All Teletype information transfers occur serially, one bit at a time.

Data Line Interface Logical Functions

The 681 controls the transmission and reception of Teletype information during subroutines entered through the program interrupt routine. Transfers occur by executing the Teletype Out instruction (TTO-6404) or Teletype In instruction (TTI-6402). Operations that occur in executing these instructions appear on engineering drawing FD-D-681-0-3. Adding these instructions modifies the flow of operations during the fetch state and adds a status (S) and character (C) state to the major state generator. These added states are entered during execution of the TTI instruction.

Teletype Out Instruction

The TTO instruction is completely executed in a fetch cycle. When memory is strobed, the instruction is read into the MB and the operation code is set into the IR. At time T1 the link is cleared and the program count is incremented by one. At time T2 the contents of the L and AC shift one position to the right and the information previously in AC11 is transmitted to the 685 on the Teletype line. Then (as in any augmented instruction) the MB clears and, if there is no break request, the computer prepares to execute the next instruction by jamming the program count into the MA, clearing the IR, and setting a 1 into the fetch state of the major state generator.

The TTO instruction is used in a program sequence that loads the Teletype character being transmitted into the AC from core memory. Then the TTO instruction is given to transmit one bit of the character (the character is rewritten in core memory). Then instructions are performed to count the character bits that have been transmitted and to determine if the last bit or last character is done.

Teletype In Instruction

The program for the TTI instruction requires three successive core memory locations. The first location contains the TTI instruction, and the two succeeding locations contain a status word (SW) and a character assembly word (CAW), respectively. A status (S) and a character (C) state are added to the major state generator for the TTI instruction. Execution of the TTI occurs in an F state, an S state, and a C state if

the instruction occurs at the correct time to receive a bit of the transmitted character. If the instruction occurs before the mid-point of a bit transmission, the reception is not effected and the instruction is completed in F and S states. All states last for the normal 1.5 μsec computer cycle.

The first cycle of the TTI instruction is a fetch state in which the instruction word is read from core memory and the next sequential core memory location is established as the address to be read during the next cycle. As in the fetch state of all instructions, memory strobe reads the TTI instruction into the MB and places the operation code in the IR. At time T1 the program count increments by one. At time T2 the MB clears, the program count jams into the MA (to set up the next location as the address for the next cycle), the program count increments by one again (PC = address of CAW), and the major state generator is set to the status state.

The second cycle of the TTI instruction is a status state in which the SW is read into the MB from core memory. Bit 0 of the SW records the active/inactive status of the selected Teletype line during the previous TTI instruction, and bits 9 through 11 of the SW serve as a real time clock to determine the sampling time for the CAW. During the S state these two units of information are sampled, operations are performed as a function of them, and they are updated and rewritten in core memory. One of the following three chains of events occurs as a function of the three possible conditions of the active/inactive status of MB0 and the contents of the real time clock.

1. If MB0=0, indicating the Teletype line was inactive during the previous TTI instruction, at time T1 the SW shifts right one position in the MB and MB0 is set to the complement of the current state of the Teletype line as an active/inactive indicator for the next TTI instruction. The program count increments by one to skip over the CAW, and the SW is rewritten in core memory. At time T2 the computer prepares to execute a new instruction as in any augmented instruction (0 $\longrightarrow$ MB, PC $\longrightarrow$ MA, 0 $\longrightarrow$ IR, and 1 $\longrightarrow$ F).

2. If MB0=1, indicating active status of the Teletype line, and MB9-11 $\neq$ 3, indicating the current character being transmitted has not reached the center of the baud for the current bit, at time T1 the SW increments by one in the MB to advance the real time clock, and the program count increments by one to skip over the CAW. The SW is then rewritten in core memory. The operations that occur during time T2 are identical to those for the previous condition (1).

3. If MB0=1 and MB9-11 =3, the center of the time baud has passed for the character being transmitted so the bit can be read. At time T1 the SW increments in the MB and

is rewritten in core memory. At T2 the machine enters the C state for the next cycle to read the bit. This preparation consists of clearing the MB, jamming the PC into the MA to establish address of the CAW for the next call on memory, incrementing the program count by one to establish the address following the CAW as the address of the next instruction, and setting the major state generator to the C state.

The third cycle of the TTI instruction is a character state entered only following an S state in which MB0 = 1 and MB9-11 = 3 (previous description for condition 3). In this cycle memory strobe reads the CAW into the MB. At time T1 the CAW shifts right one position in the MB and the bit on the Teletype line shifts into MB0. The CAW is then rewritten in core memory, and at time T2 the computer prepares to execute a new instruction as in any augmented instruction.

Note that the program is responsible for determining when a character has been completely assembled in the CAW, and for any relocation or translation of assembled characters. Characters are always assembled so that the last bit transmitted shifts into the most significant bit of the CAW and preceding bits are loaded into less significant bits of the CAW, regardless of the Teletype code or transmission path being used.

Data Line Interface Circuit Operations

The 681 option consists of a two-state addition to the major state generator of the processor and many small control circuits. The circuits of the 681 appear logically on engineering drawing BS-D-681-0-2.

Instruction Decoding

The TTO and TTI instructions used with the Type 681 Data Line Interface are special IOT instructions having a select code of 40. A logic circuit near zones 5B and 5C of the block schematic engineering drawing shows the circuit that detects these instructions to be very similar to a device selector. The circuit consists of portions of the R002 Diode Cluster module at location PD4, S111 Diode Gate at location PC5, and S107 Inverter at location PE6 connected as an 8-input negative level NAND gate with complementary outputs. This gate is enabled during the fetch state of an IOT instruction in which the select code is 40. The direct output of this gate arrives at the processor as the ground level $\overline{\text{TT INST}}$ signal to inhibit operation of the IOP generator. The IOP generator is inhibited during 681 instructions, since these instructions use the standard timing pulses of the computer rather than IOP pulses and are executed in one computer cycle rather than in a 3.75-μsec expanded cycle. The inverted output of this gate is a −3v TT INST signal level when the gate is activated. This signal enables several gating circuits within the 681 logic and arrives at the input of the Type 685 Serial Line Multiplexer as an indication that a TTO or TTI instruction is in progress.

Major State Generator Expansion

The 681 option adds a status (S) and a character (C) state to the six major states of the computer. These two states, used for execution of the TTI instruction, require two sections of the Type S284 Quadraflop module at location PC2. This module is used in the basic computer for the WC and CA states. The active and disable connections made between terminals V and H of the modules at locations PC2 and PB25 prevent entry into any state while another state is active. The S and C states are set by gated pulse amplifier circuits similar to those used in the major state generator of the processor. The S state is entered at the beginning (T2 time) of a TTI instruction (TT INST and MB10(1)). The C state is entered from an S state in which the CAW equals 4. The T2B pulse from the processor initiates entry into these states signifying the end of one instruction cycle and the beginning of the next.

TT SET, PC ⟶ MA Enable, and Special Cycle

When the processor is ready to enter either the status or the character state, the processor receives the TT SET, PC ⟶ MA ENBL, and SPEC CYCLE ground-level signals that generate in the 681. The TT SET level enables the DCD gate at the input of the pulse amplifier that produces the COUNT PC ENABLE signal. The PC ⟶ MA ENBL signal enables the DCD gate of the PA that produces the PC ⟶ MA pulse in the MA control logic. The SPEC CYCLE ground level at the major state generator prevents entry into the fetch, break, word count, or current address major states.

MB0 Shift Enable

The MB0 SHIFT ENBL (0) and (1) ground level signals connect to the enabling input of DCD gates at the 1 and 0 inputs of the flip-flop MB0. This enabling allows the MB SHIFT pulse to set or clear MB0. The circuits that produce the enabling (0) or (1) signals each consist of three 2-input negative NAND gates whose outputs connect to serve an OR function. Corresponding gates on the enable (0) or enable (1) signal serve complementary functions. A set of gates enables the 0 or 1 side of MB0 to allow shifting of the complement of the information on the Teletype line into MB0 at time T1 of the status state.

1. The Teletype line is received from the Type 685 and is made a complementary signal by inverter KJ of the S107 module at PE6.

2. A set of gates allows shifting of uncomplemented information on the Teletype line into MB0 during the character state.

3. A pair of gates set MB0 to correspond with the A-D START flip-flop of the Type 189 Analog-to-Digital Converter during the fetch state.

0 ⟶ L and RAR

During the TTO instruction the 0 ⟶ L signal level clears the link in preparation for the shifting operation that occurs at time T2. The 0 ⟶ L ground level signal enables the DCD gate that is triggered by the T2A pulse to produce the RAR signal at computer time T2. This positive RAR pulse arrives at the pulse input of gates of the accumulator that effects a 1-position rotation of the information contained in the link and the accumulator. This operation shifts the Teletype character in the accumulator one position to the right so that the least significant bit is read by the 685 option.

Shift MB and Count MB Enable

The 100-nsec T1 timing pulse of the processor combines with the status state signal in gate HJK of the R113 Diode Gate module at location PD3. The output of this gate is buffered to provide the T1S negative pulse used to produce the SHIFT MB and COUNT MB ENBL signals, and used by the skip bus in logic of the 681.

The SHIFT MB pulse is a positive pulse that triggers the DCD shift gates at the input of each MB flip-flop. This pulse produced by pulse amplifier FHJ of the S603 module at location PE15, can be triggered by three sets of conditions:

1. Diode gate HJK of the R121 module at location PC4 triggers the PA during time T1 of the status cycle if the Teletype line was inactive during the previous execution of the TTI instruction (as designated by MB0 of the SW containing a 0).

2. Diode gate LMN of the R113 module at location PB3 triggers the PA at T1 time of a character state to allow the next bit of the Teletype character to be set into the most significant bit of the CAW and the previously received bits to shift right one position.

3. The PA can also be triggered by DCD gate DE in the PA module when the A/D CONV pulse is produced in the Type 189 Analog-to-Digital Converter.

The COUNT MB ENBL signal is a positive pulse produced by a 4-input negative NAND gate composed of diode gate DEJH of the S111 module at location PC5 and expanded by segment DEF of the R002 module at location PD4. This positive pulse output triggers the PA in the MB control element that produces the COUNT MB pulse. The pulse increments the SW during the status cycle when the Teletype line has been active during the previous TTI instruction. This pulse generates when the T1S pulse occurs and the MB0 contains a 0. This gate is disabled by the SHIFT MB pulse and the two diode gate outputs that trigger generation of the SHIFT MB pulse.

Skip Bus In

The SKIP BUS IN positive pulse connects to the normal IOS interface connector of the PDP-8 to cause a pulse amplifier to produce the COUNT PC ENABLE pulse. The SKIP BUS IN pulse increments the program count to skip over the CAW to the next instruction. It occurs each time a T1S pulse is produced unless inhibited by the condition in which the real time clock of the SW contains a count of 3. The pulse is produced by the DEF diode gate of the R121 module at location PC4, is inhibited by diode gate LMNT of the R121 module at location PC4, and is latched by diode gate LNK of the S111 module at location PC5.

CHAPTER 4

CORE MEMORY

The PDP-8 core memory performs data and instruction storage and retrieval. The basic PDP-8 comes with a 4096-word, 12-bit core memory. Core memory capacity can be expanded by increments of 4096 words to a maximum of 32,768 words. Memory expansion requires the use of Type 184 Memory Modules and a Type 183 Memory Extension Control. The basic method of accessing any individual location within a 4K memory array applies to any size memory. The description of the Type 183 Memory Extension Control discusses methods of selecting the appropriate 4K array.

MEMORY ORGANIZATION

The 4K memory module used in the standard PDP-8 is a simple, coincident-current, ferrite-core array assembled from core planes 64 cores wide by 64 cores deep. Each plane operates by read, write, and inhibit currents originating in transistor power supplies and gating circuits. Figure 4-1 shows the interrelationship of the elements which constitute the core memory system. The memory data register (MB) and the address selection register (MA), located in the processor, are described in detail in Chapter 3 of this manual.

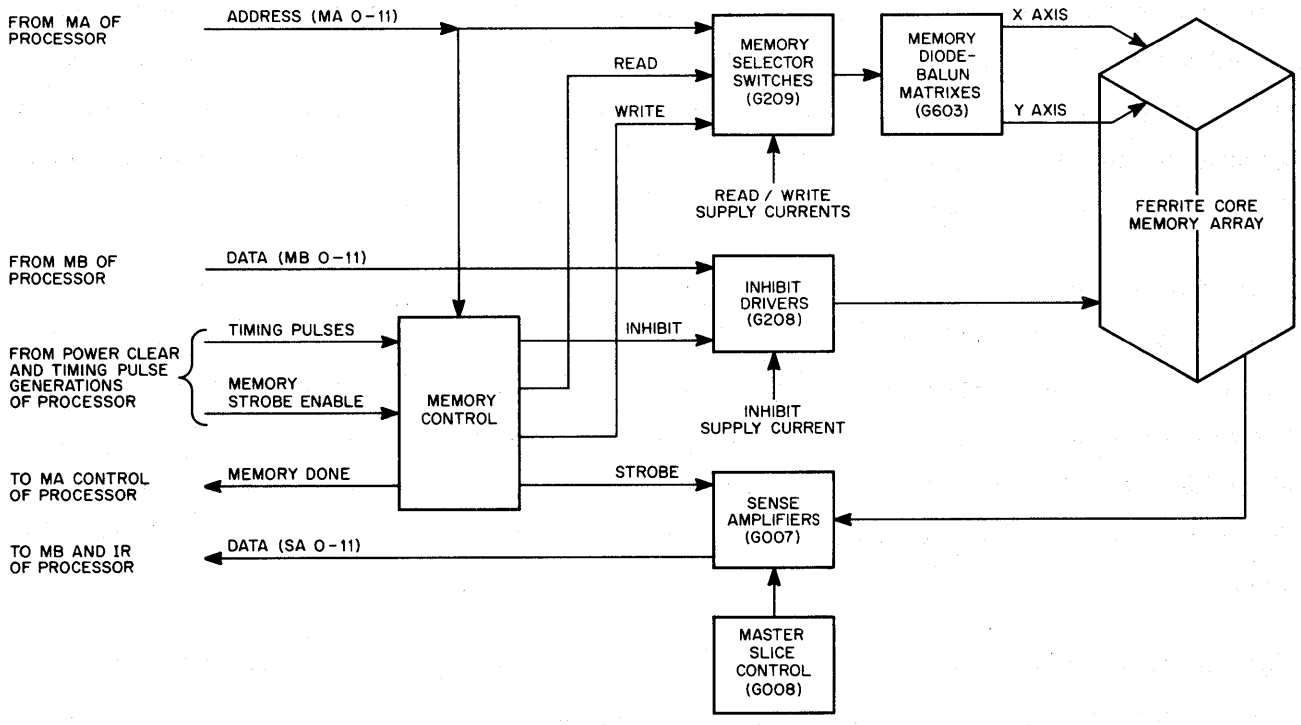


Figure 4-1 Core Memory System, Block Diagram

Ferrite-Core Memory Array

The ferrite-core memory array consists of 12 planes, each having 4096 ferrite cores arranged in a square 64 by 64. Each core can assume either of two stable magnetic states corresponding to binary 1 and binary 0. Each core is traversed by four windings. An X-axis read/write winding passes through all the cores in one horizontal row; a Y-axis read/write winding passes through all the cores in one vertical row; a sense winding and an inhibit winding pass through all the cores of each plane.

To clarify the description of memory operation, Figure 4-2 shows a simple 4 by 4 core plane. Note that a current passing from right to left on the X2 winding (write direction) produces a magnetic field that tends to change all the cores in that horizontal row from the 0 to the 1 state. However, this current is insuffient to cause the change and is known as the half-select value. Passing a current from top to bottom of the Y3 winding produces a similar effect on all the cores in that vertical row. Note, however, that there is one core, at the intersection of the X2 and Y3 rows, through which both currents pass. Since the X and Y write currents are turned on simultaneously, the magnetic fields are mutually reinforcing and their combined (full-select) strength causes this, and only this, core to change state to the 1 condition. In the PDP-8 core memory, the twelve planes have all their X1 windings connected in series, all their Y1 windings connected in series, and so on. Thus, each plane is equivalent to one bit of a 12- bit storage cell. If X2 and Y3 write currents flow, the X2Y3 core on each of the twelve planes changes to the 1 state.

If the storage cell consisting of twelve X2Y3 cores contains 0's as well as 1's, the cores in those planes which correspond to 0 bits cannot change state when the X and Y write currents flow because a current passes in the read direction through the inhibit winding of each 0 plane. Although the X2Y3 address drive lines in each 0 plane still receive full-select currents, the current in the inhibit winding produces an opposing magnetic field equivalent to that from a half-select read current. The effective write flux, therefore, reduces to half-select value and the core does not change state.

To read information contained in the X2Y3 cell, read currents (of opposite polarity to the write currents) pass to the X2 and Y3 windings in each plane. All cores of the X2Y3 cell then change to the 0 state, except those cores inhibited during writing and already in the 0 state. The windings are so positioned on the core that full-select read currents induce only a small signal into the sense winding of planes in which the X2Y3 core is already in the 0 state. However, in any plane where the X2Y3 core changes from 1 state to the 0 state, the resulting flux change induces a relatively large signal into the sense winding of that plane.

After amplification and reshaping, these binary 1 pulses complete the information transfer by setting the corresponding MB flip-flops. Reading a memory cell destroys the information in it; therefore, a read

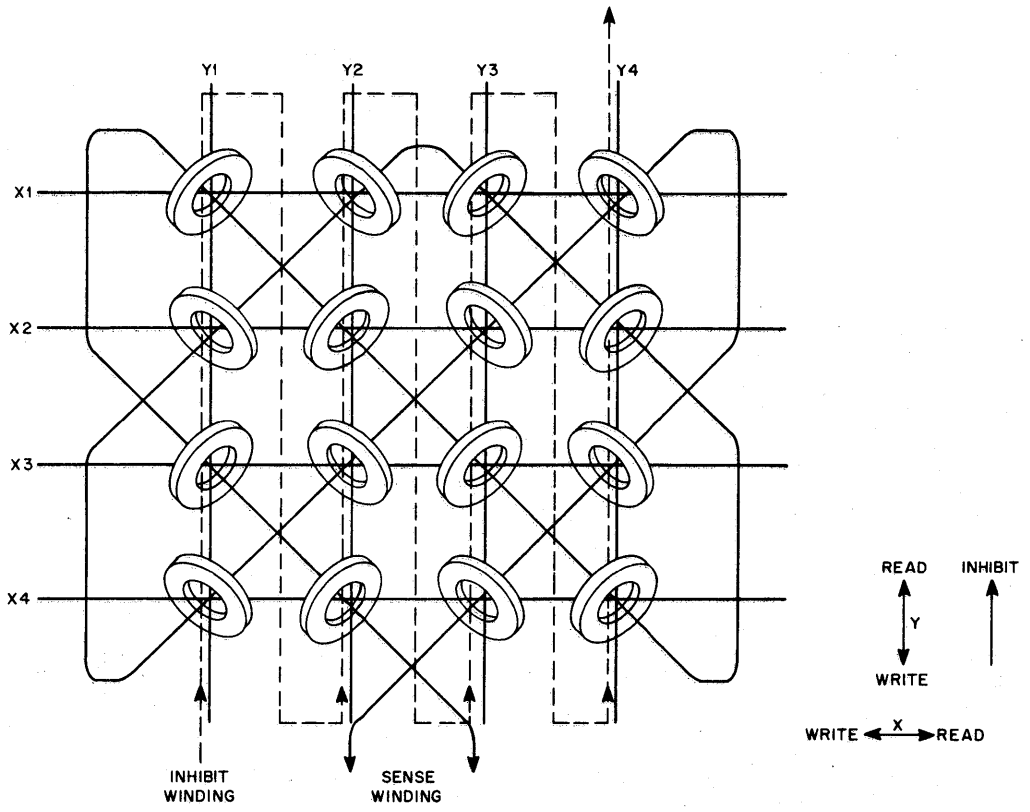


Figure 4-2 Simple Core Memory Plane, Showing Read/Write Sense, and Inhibit Windings

operation which transfers information from ferrite cores to the MB is immediately followed by a write operation which rewrites the information from the MB into the memory cell. The MB stores the information until deliberately cleared by the control logic circuits of the processor.

Address Selection

Any one of the 4096 locations in the PDP-8 memory requires twelve address bits for complete specification. However, since the registers of the processor can accommodate only twelve bits, a complete address cannot be used as part of a memory reference instruction word (in which the first three bits must specify the operation to be performed). Therefore, the PDP-8 memory is organized into 32 pages (or blocks), each containing 128 consecutive memory locations. These pages are numbered 0 through 37_8. Specification of any one of 128 locations within a page, which is accomplished by bits 5 through 11 of a memory reference instruction requires only 7 bits. With the operation code held in bits 0 through 2, bit 3 designates indirect addressing of any location in memory, and/or bit 4 selects the current page or page 0 as the location of the page address contained in bits 5 through 11.

Suppose, for example, that the program starts (and is largely contained) in some page which we will call "K". When the starting address is loaded by the manual keys and switches and sets bits 0 through 4 of

the PC to specify page K, memory reference instructions need specify only the seven least significant bits of the address of each operand in page K. Such instructions contain a 1 in bit 4 to denote that the operand is located in the same page (called the current page) as the instruction. By placing a 0 in bit 4, a memory reference instruction can also address any location in page 0. Thus, any memory reference instruction can directly address 256 locations, 128 of which are in the current page, and the other 128 in page 0. A directly addressed instruction requires two cycles: the instruction is retrieved from core memory during the fetch cycle; the directly addressed operand is retrieved and the operation is performed during the subsequent execute cycle. The simplified flow chart in Figure 4-3 illustrates the sequence of events.

Extracting an operand from a location not in the current page or in page 0 requires the full 12-bit address. This is accomplished by inserting a 1 in bit 3 of the memory reference instruction, to denote indirect addressing. Bits 5 through 11 of the instruction word then contain the address of a memory cell (in the current page or in page 0) which contains the 12-bit absolute address of the operand. The execution of an indirectly addressed instruction requires three cycles. During the fetch cycle, the instruction word is retrieved from memory and the operation code is set into the IR. A defer cycle follows, in which the absolute address of the operand is retrieved from a memory location in page 0 or the current page and is set into the MA. Finally, during the execute cycle, the operand itself is retrieved from a location in any page, and the instruction is executed.

Memory Selector Switches and Matrixes

The memory selector switches decode the address specified by the MA and select Y and Y drive lines and X and Y ground lines in the associated matrixes. The application of a read or write signal generated in the memory control determines the direction of current through the cores of the addressed cell by causing the switches to select either read drive and read ground lines, or write drive and write ground lines for each axis. Figure 4-4 shows a simplified diagram of the selection process for the Y axis only. In this figure, only the selected diode-balun network of the Type G603 module and the four selected switches of the Type G203 module at locations MC12 and MD12 are shown. If the MA addresses cell X00Y00 and a READ signal occurs, the Y drive selector switch (Q12) connects the Y00 read drive bus to the positive output of the read/write current power supply, through the current determining resistor, and the Y ground selector switch (Q15) connects the Y00 read ground bus to the negative output of the read/write current supply. Current (determined mainly by the 80-ohm resistor and the power supply voltage) then flows from the read drive bus through diode D7, the balun, core Y windings, and diode D16 to the read ground bus. Conversely, if a WRITE signal occurs, the write drive bus connects to the positive supply (through Q16) and the write ground bus connects to the negative supply terminal (through Q9). Current then flows

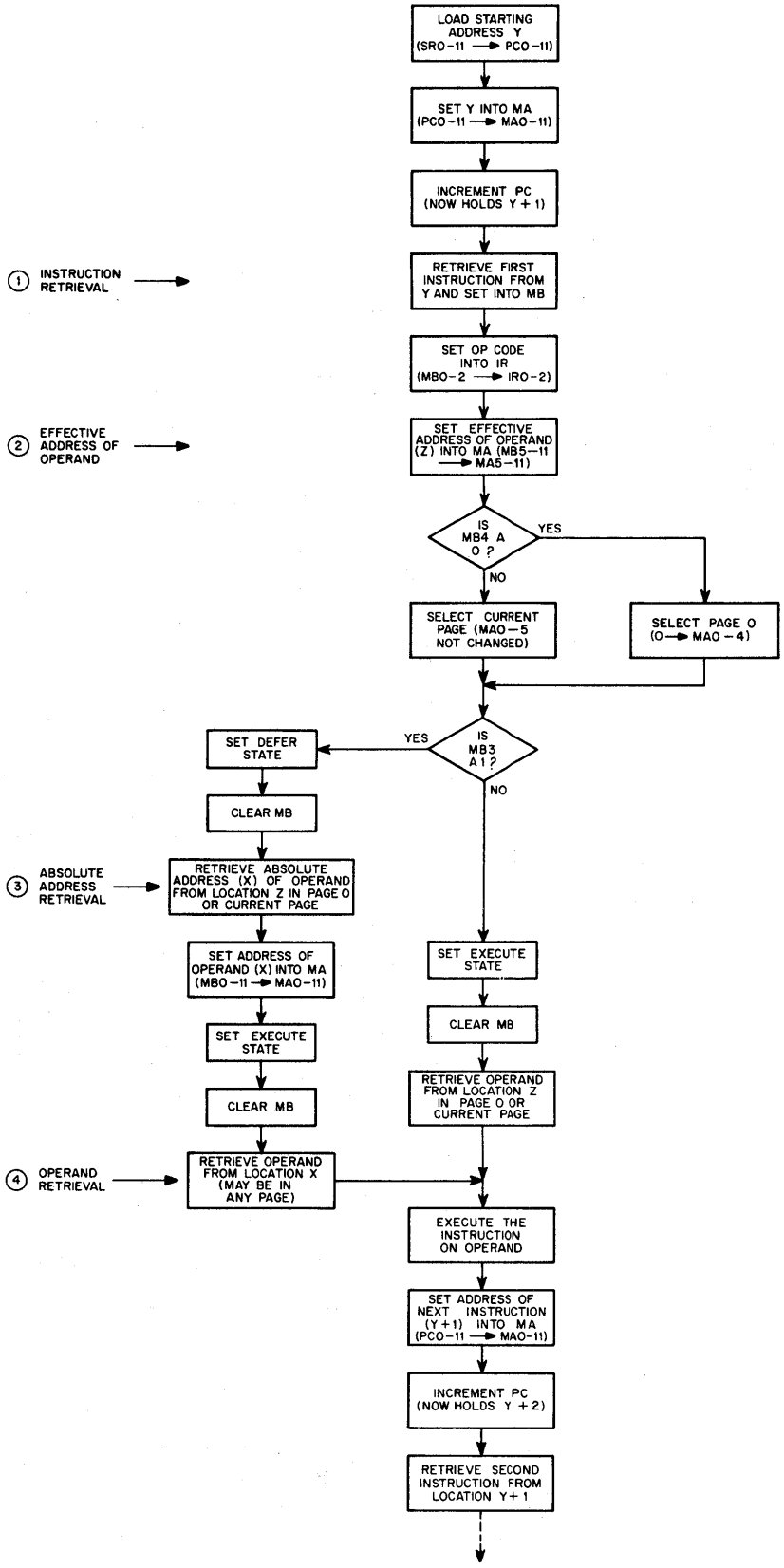


Figure 4-3 Direct and Indirect Address Selection, Simplified Flow Chart

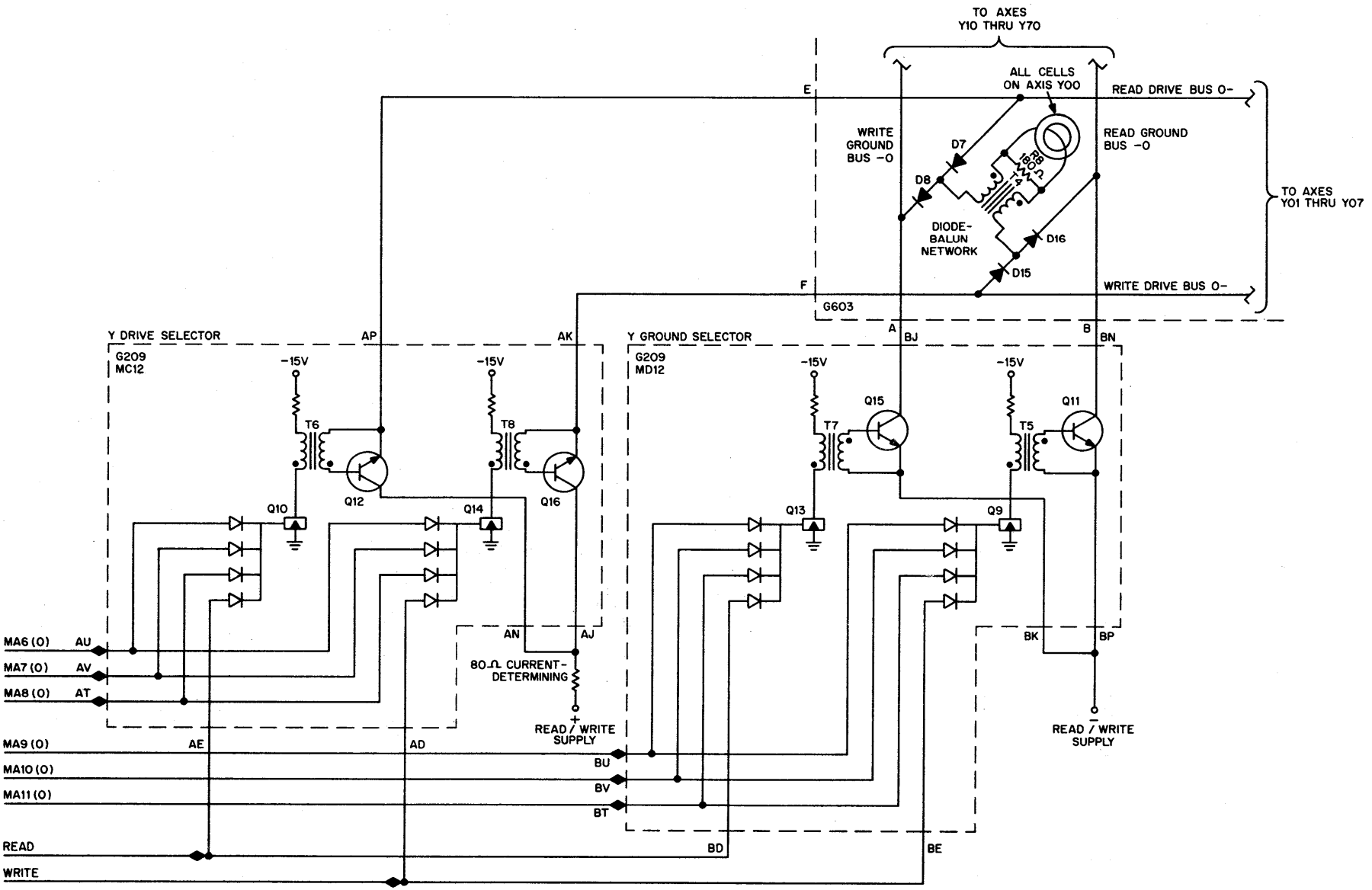


Figure 4-4 Read/Write Current Generation and Flow Path

from the write drive bus through diode D18, the balun, and core windings (in the opposite direction) and thence through diode D8 to the write ground bus. Switching both the drive bus and the ground bus, and the use of the diode-balun network permits the core windings to be balanced with respect to ground. The resulting reduction of stray inductance and capacitance permits a substantial increase in the operating speed of the memory.

Inhibit Drivers

An inhibit driver exists for each plane of the array. During a write operation, an INHIBIT signal generated in the memory control arrives at all inhibit drivers. Each driver also receives a signal denoting the state of the corresponding bit of the MB. Inhibit drivers which receive a signal denoting a 0 state in the MB bit are gated on and cause inhibit current to be applied to the associated plane of the memory array.

Sense Amplifiers and Master Slice Control

During a read operation, the signal induced on the sense winding of a core plane by a core changing state is on the order of 50 mv. In planes where a core does not change state, some noise is generated (having an amplitude of a few millivolts). The sense winding of each plane is connected to a sense amplifier which samples the current induced on the winding and produces standard pulses to transfer information into the MB reliably. The sense amplifier raises the signal to a level capable of triggering a pulse amplifier to produce a standard positive pulse. During the carefully timed MEM STROBE pulse applied to the sense amplifier by the memory control, the core output signal is compared with a preset reference level generated by the master slice control. An output pulse occurs only if the amplified signal exceeds the reference level at strobe time. Signals due to a change of core state meet this condition, whereas amplified noise does not. Thus the sense amplifiers generate output pulses of standard amplitude and duration which set MB flip-flops only when reading a binary 1 in the associated planes.

Memory Control

The memory control contains the flip-flops, delay lines, and gating circuits which produce the levels and pulses required for correctly timed memory operation. A MEMORY START signal, generated in the computer timing circuits, initiates the read operation. This pulse sets the MEM ENABLE and READ flip-flops and generates the MEM STROBE pulse which causes the sense amplifiers to sample the core plane signals when read current reaches peak amplitude. Timing pulse T1, also generated in the computer timing circuits, initiates the write operation by setting the WRITE and INHIBIT flip-flops. At the end of the write operation, all memory flip-flops clear in preparation for a new cycle. Memory control also inhibits generation of the MEM STROBE pulse during the execute cycle of DCA and JMS instructions and during the

inward transfer of information in a data break. Under these conditions, the cores receive information stored in the MB during the previous cycle. The memory strobe is therefore suppressed, so the read operation serves to clear the selected core memory cell.

DETAILED CIRCUIT OPERATIONS

Memory Selectors and Memory Selector Matrixes

The Type G209 Memory Selector modules decode the information contained in the MA to perform cell selection and turn on read/write currents in response to gating signals supplied by the memory control. The Type G603 Memory Selector Matrix modules contain the read and write drive and ground lines, the diodes, and the baluns. Address bits MA0 through MA5 select read and write lines in the matrix of the X-axis; bits MA6 through MA11 select read and write lines in the matrix of the Y-axis. Engineering drawing BS-D-8M-0-12 shows the logic circuits for X-axis selection, and drawing BS-D-8M-0-13 shows those for Y-axis selection. The following description refers to the Y-axis drawing.

Drive selector switches in the four Type G209 Memory Selector modules located in MC12 through MC15 and MD12 through MD15 decode address bits MA6 through MA8. These circuits in the top half of the double-height modules appear at the left of the drawing. They connect the positive line of the read/write power supply to one of the read or write drive lines of the matrix, through a current-determining resistor. Ground selector switches in the bottom half of these modules decode address bits MA9 through MA11. These circuits, along the bottom of the drawing, connect one of the read or write ground lines to the negative line at the read/write power supply.

Figure 4-4 is a simplified logic diagram showing the internal logic of the selector. Each Type G209 module contains the logic for selecting a read drive line and a read ground line or a write drive line and a write ground line for one of two addresses (eight switches per module). A 4-input diode gate controls each switch. The MA assertion levels flow to the diode gates to determine the drive selector and ground selector to be operated. If a negative READ level arrives at gate Q10, a surge of current through pulse transformer T6 turns on transistor Q12, connecting the positive read/write supply line to the read drive line selected. Similarly, in the lower half of the module, the same address lines turn on gate Q13 and transistor Q15 connecting the selected read ground to the negative read/write supply line. If a WRITE level arrives at gate Q14, transistor Q16 turns on to connect the selected write drive line to the read/write supply, and gate Q9 and transistor Q11 turn on to connect the selected write ground line to the read/write supply.

In each axis, four Type G603 Memory Selector Matrix modules pass the read/write currents between the G209 modules and the drive lines of the core array. Each G603 module contains 16 diode-balun networks.

On engineering drawings, the drive lines appear in horizontal pairs, of which the upper is read and the lower is write. The ground lines appear as vertical pairs, of which the left is the write ground and the right is the read ground. Four diodes and a balun connect at each intersection of a read and a write pair (the drawing shows only those at the ends of the lines). The diodes isolate the read and write current paths from each other; the baluns balance the core windings with respect to ground.

Inhibit Drivers

The PDP-8 memory system utilizes six Type G208 Inhibit Driver modules, in location MC21, MC22, MC24, MD21, MD22, and MD24. If the system is equipped with the Type 188 Memory Parity Option another G208 module is added at location MC25 for the parity bit. Each module contains two inhibit drivers, providing a total of twelve drivers, one for each bit of the MB (or one for each core plane). Engineering drawing BS-D-8M-0-15 shows the logic of the inhibit drivers, and engineering drawing RS-B-G208 is a schematic of an individual driver module. Each driver consists of a 2-input negative NAND gate, transformer-coupled to a transistor switch. The negative 0 level of the corresponding MB flip-flop conditions one input of the gate. When the negative 1 level of the INHIBIT flip-flop arrives at the second input of the gate, the gate turns on its associated inverter. The transition occurring at the inverter output turns on a transistor switch that permits inhibit current to flow in the associated plane. An 80-ohm current-determining resistor connects between the positive inhibit current supply line and the transistor switch of each inhibit driver. This resistor and the voltage of the inhibit power supply mainly determine inhibit current amplitude in establishing a value equivalent to a half-select read current.

Sense Amplifiers and Master Slice Control

The PDP-8 memory contains twelve Type G007 Sense Amplifiers and one Type G008 Master Slice Control. Twelve of the sense amplifiers supply a standard positive pulse to the MB when an associated memory core changes from the 1 state to the 0 state during a read strobe operation. A 13th sense amplifier supplies a parity bit when the Type 188 Memory Parity option is in use. The master slice control supplies all the sense amplifiers with closely controlled reference voltages used in the clamping and comparator stages. Drawings RS-B-G007 and RS-B-G008 contain schematic diagrams of the sense amplifier and master slice control, respectively. Engineering drawing BS-D-8M-0-15 shows the connection of these modules in the memory system.

The sense amplifier contains a 2-stage dc preamplifier, a rectifying slicer, and a gated pulse amplifier. The first stage of the dc preamplifier is a difference amplifier utilizing two transistors enclosed in a common case. The sense winding of the associated core plane connects between the two transistor bases. Signals induced on the sense winding are amplified and appear as a push-pull output at the collectors of the double transistor. The second preamplifier stage (also a difference amplifier), further amplifies the

output which then arrives at the rectifying slicer. If the signal level at the slicer exceeds the slice potential applied by the master slice control, it enables the output gate. The slicer suppresses noise induced into the sense winding of a memory plane by the read current pulses. Therefore, only the much larger signal produced by a core changing state enables the output gate.

A MEM STROBE pulse, 40 nsec wide, arrives at the sense amplifier output gate. This pulse, generated by the memory control circuits, is precisely timed to occur when read currents have reached their peak amplitude. It is at this moment that a core which is changing state produces the most rapid change of flux and therefore induces the largest signal on the sense winding. When the strobe pulse arrives at a gate enabled by a core changing state, the gate produces a standard 100-nsec positive output pulse which sets the corresponding flip-flop of the MB.

The master slice control contains three Zener diode reference voltage networks, each with an associated emitter-follower output voltage control. The 1ST STAGE CLAMP level signal flows to the input difference amplifier; the 2ND STAGE CLAMP level signal reaches the second stage of the sense amplifier; and the SLICE LEVEL signal arrives at the rectifying slicer. The 1ST STAGE CLAMP level is a fixed potential; an adjustment potentiometer varies the other two levels. The SLICE LEVEL signal is normally adjusted so that the sense amplifiers give symmetrical deviations when the +10v supply varies to the upper and lower marginal levels.

Memory Control

Memory control generates control levels and pulses necessary to operate the memory. Engineering drawing BS-D-8M-0-15 shows the logic and Figure 4-5 a timing diagram. The chief elements of the memory control are the flip-flops, the read and write delay lines, and pulse amplifiers.

A single Type B204 module in location MD16 contains the unbuffered MEM ENABLE, READ, WRITE, and INHIBIT flip-flops. At power turnon, POWER CLEAR pulses from the processor timing circuits clear all four flip-flops. A MEMORY START signal, also generated in the processor timing circuits, leaves processor logic at terminal PF1E and enters memory logic at terminal MF36E. This positive pulse sets the MEM ENABLE and READ flip-flops and reaches the double-height Type W300 Delay Line module in location MC17/MD17. This delay line has two outputs. After a 100-nsec delay, the output appears at terminal DN, and flows to a gate in module MD19. If already enabled by a negative MEMORY STROBE ENABLE level at terminal MD19E, the gate gives an output and triggers pulse amplifier DEF in module MC20. The negative pulse at terminal MC20D arrives at the delay line and pulse amplifier in module MD20. The MEM STROBE negative pulse appears at terminal MD20N, 250 to 350 nsec after the leading edge of the

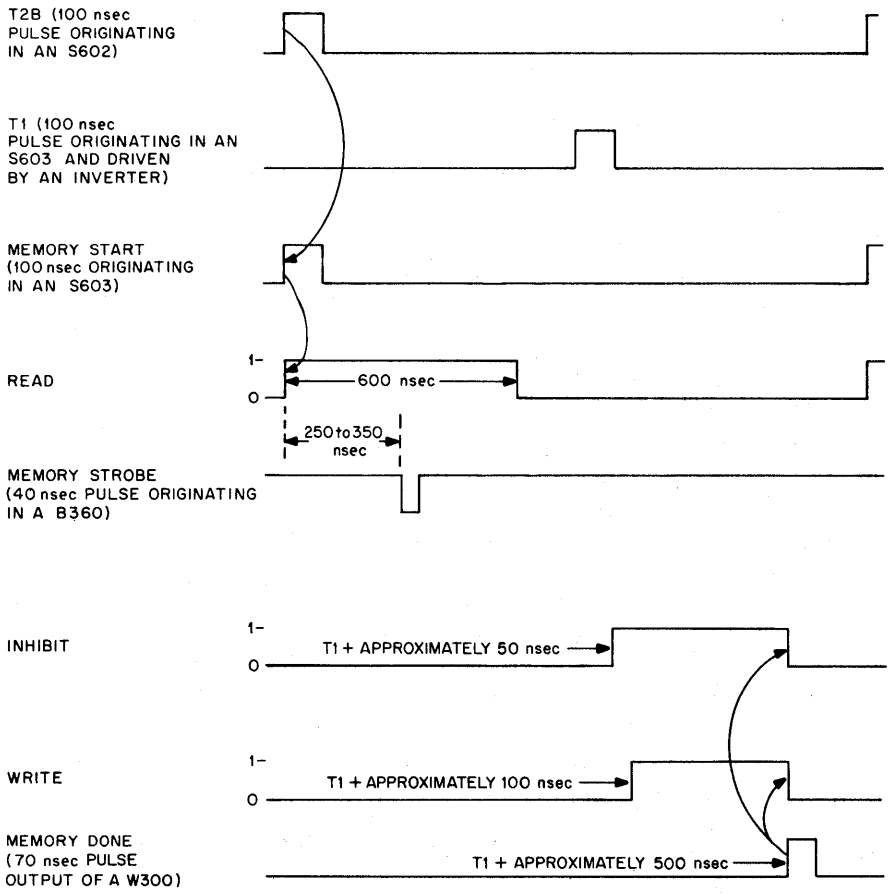


Figure 4-5 Memory Timing Diagram

MEMORY START pulse. The second output of the Type W300 Delay Line appears at terminal MD17DT after a delay of 600 nsec, and resets the READ flip-flop. The negative READ (1) level flows to a Type B684 Bus Driver in location MC16, and the buffered READ level appears at terminal MC16D for distribution to all of the G209 modules.

Timing pulse T1 initiates the write operation, entering memory control at terminal MF36F and triggering pulse amplifier NPR in module MC20. The negative pulse at terminal MC20N reaches a 2-inverter NAND gate in module MD19. If enabled by the MEM ENABLE (1) level, the gate gives a pulse output which amplifies and flows to a second Type W300 Delay Line located in module MC18/MD18. This delay line gives three outputs. The first, which occurs after a delay of 50 nsec, sets the INHIBIT flip-flop. The second output occurs after a delay of 100 nsec and sets the WRITE flip-flop. The WRITE (1) level reaches a bus driver, and the negative WRITE level arrives at terminal MC16N for distribution to the memory selectors. The third output of the delay line appears at terminal MD18T, after a delay of 500 nsec, triggers a pulse amplifier in module MC19, and supplies a MEM DONE pulse to the MA control of the processor. The negative pulse which reaches terminal MC19U clears all four memory control flip-flops.

Current Source

The Type 708 Power Supply provides all power necessary for operation of the memory array and memory logic as well as for the processor logic. This unit contains three independent power sources: an unregulated logic supply which produces +10v and -15v; a floating supply which provides 40 vdc and feeds two independent regulators for the read/write and inhibit currents, respectively; and a variable marginal check supply. A schematic diagram of the power supply is in engineering drawing RS-C-708.

Unregulated +10v and -15v Supplies

A tapped winding on the power transformer energizes a full-wave rectifier circuit producing the unregulated +10 and -15v supplies. This ferroresonant regulating transformer delivers a constant output voltage over a considerable range of input voltage variation. To eliminate ripple and load transients, 210,000 μf of filter capacitance exists for the -15v supply, and 105,000 μf for the +10v supply. The storage capability of these filters allows the computer to tolerate short-duration transient interruptions of the primary power supply lasting as much as 50 msec.

Marginal Check Supply

A variable transformer (which connects to an independent secondary winding of the power transformer) and a half-wave rectifier and filter capacitor provide a voltage source variable between 0 and 20 vdc. A meter permits accurate voltage setting, and a DPDT switch permits connection of the supply to produce either a positive or a negative output (with respect to ground). The maximum current output of the marginal check supply is 2 amp, and the maximum ripple voltage is 700 mv p-p. The output of this supply may replace the normal unregulated +10 and -15v supplies in any row of modules for maintenance tests.

Inhibit Supply

A full-wave rectifier circuit, from an independent winding on the power transformer, provides 40 vdc (floating) for the inhibit and read/write supplies. A 34,400 μf filter capacitance eliminates major ripple and load transients. Series regulator transistor Q1, which receives a control voltage from a Type G808 Power Supply Control module, regulates the filtered supply. Contacts of relay K1 in the positive inhibit regulated supply line disconnect the supply from the memory system until all voltages are at correct operating levels. The regulated inhibit supply has an output voltage adjustment range of 27.0 to 37.0v, at an output current of 1 amp. Under these conditions, ripple is less than 50 mv and regulation is better than ±0.5% over the entire adjustment range. The maximum permissible output current is 2 amp.

Read/Write Supply

Series regulator transistor Q2, which receives its control voltage from a second Type G808 Power Supply Control module, regulates the read/write supply which comes from the same filtered supply as the inhibit supply. The characteristics of the read/write regulated supply are identical to those of the inhibit regulated supply, except for the maximum current rating, which is 1.5 amp.

Power Supply Control G808

The Type G808 Power Supply Control module is a preamplifier for the inhibit or read/write series regulator in the Type 708 Power Supply. A schematic diagram of the control unit appears in engineering drawing RS-B-G808. The reference element is a Zener diode, which permits better than 0.25% combined line and load regulation over the voltage adjustment range.

In addition to the usual regulating functions, the control provides voltage compensation as a function of memory array temperature. A positive-coefficient thermistor, having a resistance of 350 ohms at 25°C, is within the memory array. The control unit senses the resistance of this thermistor and causes output voltage to be reduced as array temperature rises. The temperature tracking coefficient is approximately −0.5% per degree C, when carborundum thermistor A0905P-8 is used.

The control unit provides a −3v level as a function of correct output voltage. Terminal AD of the control is the sensing input. When terminal AD senses a voltage that is within 3v of the designated regulator output voltage, a −3v OK level signal appears at terminal AF of the control. When the voltage at terminal AD differs by more than 3v from the designated value, terminal AF reaches ground potential. Note that in both the inhibit and read/write power supplies, sensing terminal AD connects to the memory side of the contacts of relay K1. Thus, until relay K1 is energized, no OK signal appears at terminal AF.

Relay Driver G809

The Type G809 Relay Driver module senses the potential of the −15v supply line after power turnon and energizes relay K1 when the line potential reaches −14v. The relay contacts then connect the inhibit and read/write supplies to the memory system. The relay driver produces a −3v OK signal at terminal R whenever the relay is energized. If the −15v line drops below −14v for any reason, the relay de-energizes, thereby disconnecting the read/write and inhibit supplies from the memory system, and terminal R rises to ground potential.

The OK levels produced by the inhibit supply control, the read/write supply control, and the relay driver join and route to the processor run control. If any one of these OK levels disappears, the OK line is grounded and the computer program halts. A schematic diagram of the relay driver is in engineering drawing RS-B-G809.

TYPE 183 MEMORY EXTENSION CONTROL

Adding 4096-word core memory fields (Type 184 Memory Modules) extends the storage capacity of the PDP-8 beyond the 4096 words of standard core memory. The addition of seven fields yields the maximum storage capacity of 32,768 words. The Type 183 Memory Extension Control provides field select control

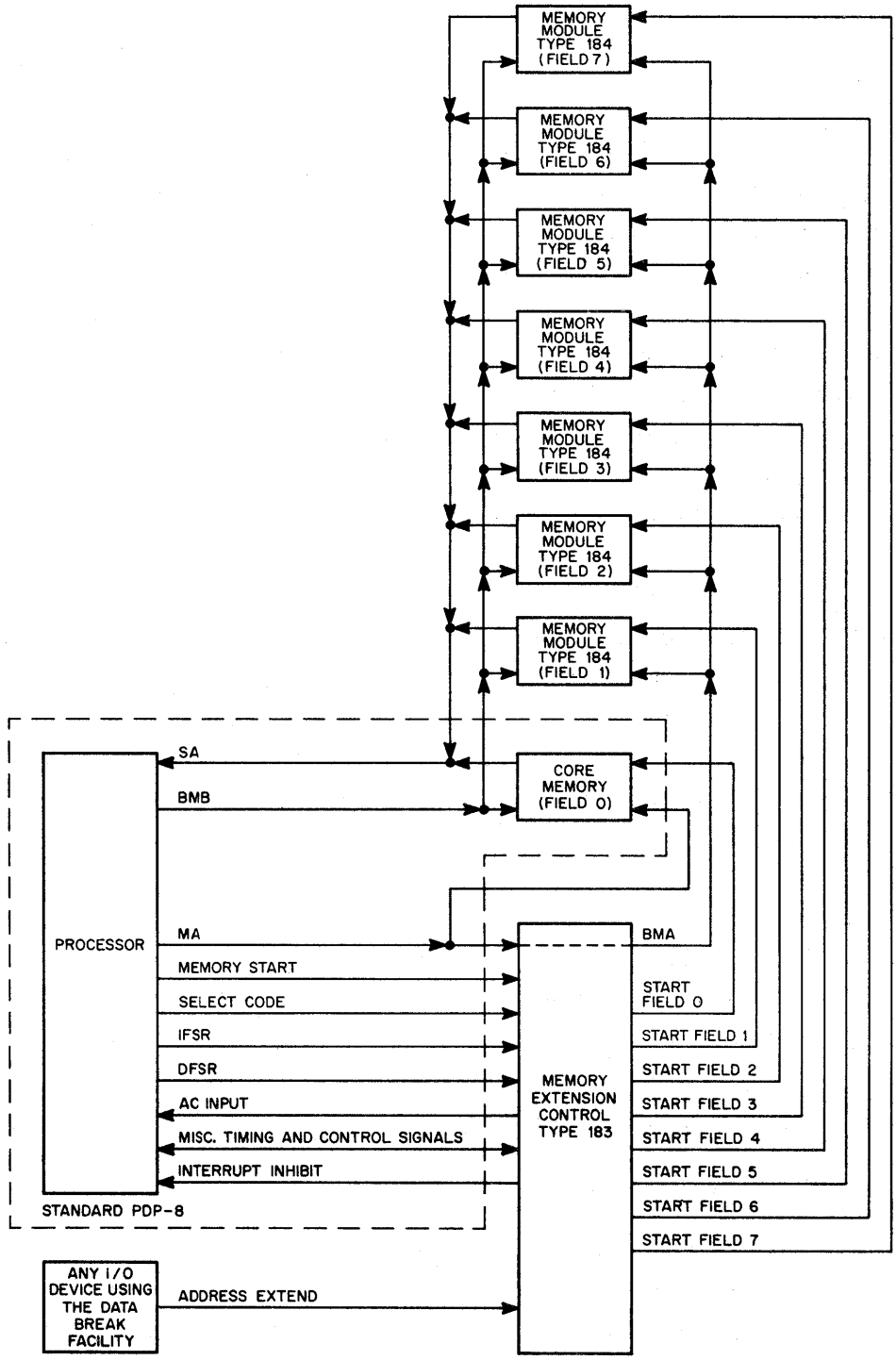


Figure 4-6 Extended Memory, Basic Block Diagram

and address extension control for the Type 184 Memory Modules. The organization of an extended memory system of the PDP-8 appears in Figure 4-6. This figure also indicates the interface and signal relationship between elements of the memory extension and the basic PDP-8.

Block Diagram Discussion

Direct addressing of 32,768 words requires 15 address bits. However, since the PDP-8 already has direct and indirect addressing procedures within the standard core memory, a field can be program-selected and all 12-bit addresses are assumed within the selected field.

Memory extension control consists essentially of several 3-bit registers that extend addresses to establish or select one of the eight possible fields. A START FIELD pulse that initiates operation of an appropriate memory field for each memory cycle produces this selection. Field selection occurs differently for instruction, retrieval, programmed data access, and data break information access. The standard memory of the PDP-8 is field 0; additional memory modules are fields 1 through 7. The block diagram of Figure 4-7 shows the principal functional circuit elements of the memory extension control and the relationship of these elements to each other, to the processor, and to additional memory modules.

Instruction Field Register (IF)

The instruction field register is a 3-bit register that determines the memory field which contains the instructions of a program. Operating the LOAD ADD key clears the IF, then sets it by a transfer of 1's from INST FIELD switch register. During the execution of a programmed JMP or JMS instruction, a jam-transfer of information in the instruction buffer register sets the IF. During a program interrupt, the save field register automatically saves the original contents of the IF for later restoration to the IF from the instruction buffer register at the conclusion of the subroutine.

Data Field Register (DF)

The data field register is a 3-bit register which determines the field to be used for data storage and retrieval. Initially, the register is cleared and then set by a transfer of 1's from the DATA FIELD switch register by operation of the LOAD ADD key. During execution of the program, a CDF (Change to Data Field N) instruction loads the DF with the selected field number by a jam-transfer from bits 6 through 8 of the MB. All subsequent memory requests for operands automatically go to field N until a new CDF instruction is executed. During a program interrupt, the current contents of the DF are automatically stored in the save

field register. At the conclusion of the program interrupt subroutine, an RMF (Restore Memory Field) instruction jam-transfers the contents of the save field register back into the IF and DF.

Instruction Buffer Register (IB)

The 3-bit instruction buffer register serves as an input buffer for the IF. All programmed transfers of information into the IF come through the IB; however, manual transfers from the INST FIELD switches route directly into the IF as well as into the IB. A CIF (Change Instruction Field) instruction loads the IB with

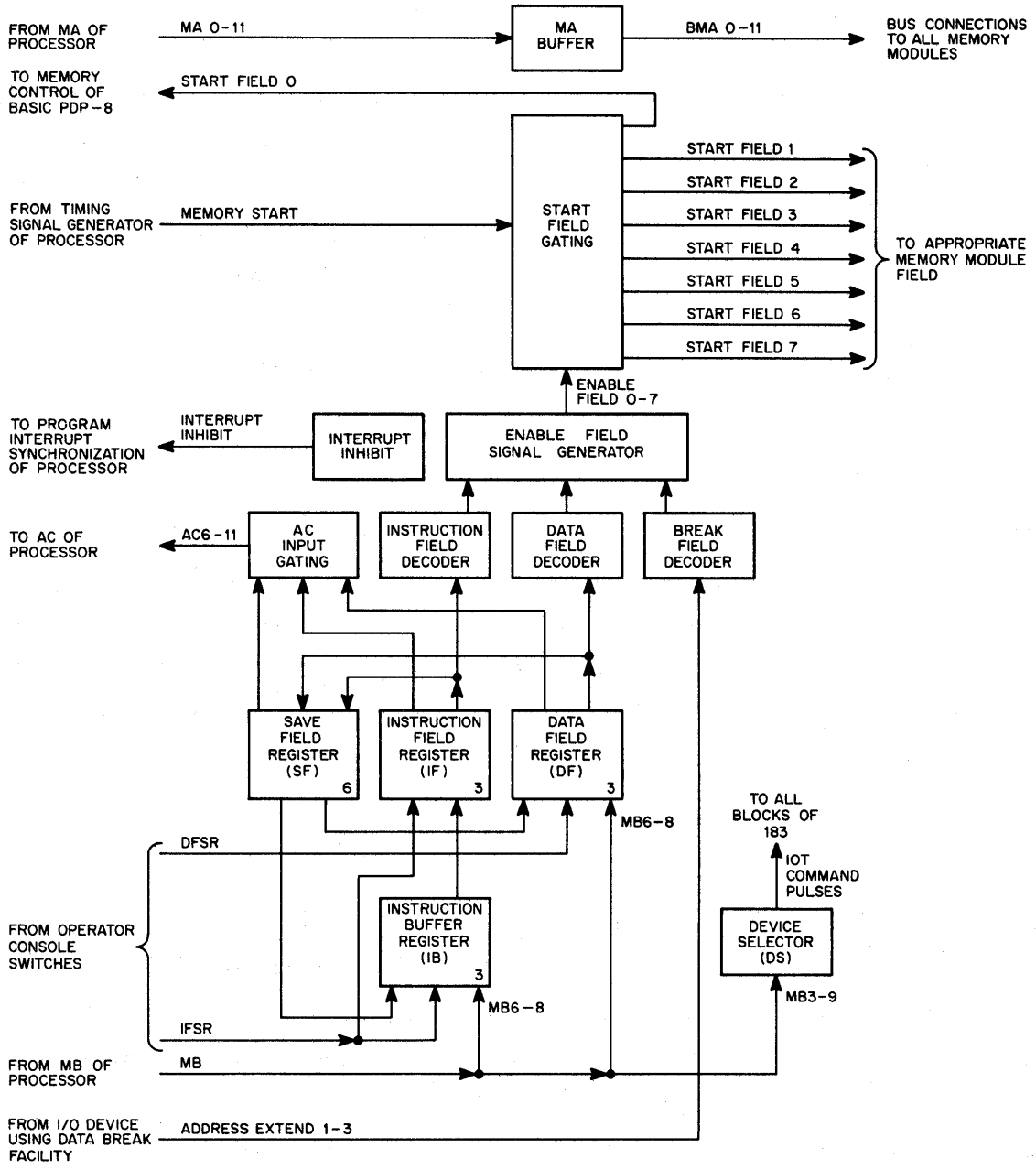


Figure 4-7 Memory Extension Control, Block Diagram

the field number in bits 6 through 8 of the MB. An RMF instruction at the conclusion of the program interrupt loads the IB with the original contents of this register, which was temporarily stored in the save field register during the interrupt.

Save Field Register (SF)

The 6-bit save field register provides temporary storage for the contents of both the IF and DF. When a program interrupt occurs, the SF is first cleared and then loaded from the IF and DF. The program may then load these registers with the field numbers in which the subroutine operates. At the conclusion of the subroutine, an RMF instruction loads the contents of the SF0 through SF2 into the IB for transfer into the IF, and loads the contents of bits SF3 through SF5 into the DF.

Field Decoders and Enable Field Signal Generator

Signals produced by three binary-to-octal decoders operate the ENABLE FIELD signal. The break decoder receives a B SET enabling signal from the major state generator of the processor and three address extend signals from the device using the data break. When the instruction is not a JMP or a JMS, the processor produces the E SET signal, enabling the data decoder which decodes the six complementary outputs of the DF. When both the break decoder and the data decoder are disabled, the instruction decoder receives an enabling signal to decode the output of the IF. Only one decoder at a time can be enabled. Each decoder, when enabled, produces one of the eight possible ENABLE FIELD signals determined by the bit combination applied to its input.

Start Field Gating

Each field is a memory system equipped with address selectors, inhibit selectors, and a memory control. The MEM START pulse goes to the selected field through the start field gating. The MEM START pulse arrives at eight DCD gates simultaneously. However, the ENABLE FIELD level conditions only one of these gates at a time.

The output of the conditioned DCD gate triggers a pulse amplifier, producing a START FIELD pulse. This pulse sets the MEM ENABLE flip-flop in the associated memory field and starts the read cycle only in that field whose MEM ENABLE flip-flop was set by the START FIELD pulse.

Accumulator Input Gating

The accumulator input gating transfers the contents of the SF, IF, or DF into the AC. The gating circuits sample the contents of registers and supply positive setting pulses to the AC flip-flops after receiving

command pulses from the device selector gates. An RIB (Read Interrupt Buffer) instruction sets the contents of the SF into bits 6 through 11 of the AC. An RIF (Read Instruction Field) instruction sets the contents of the IF into bits 6 through 8 of the AC. An RDF (Read Data Field) instruction sets the contents of the DF into bits 6 through 8 of the AC. All transfers take place during time state T1 of the fetch cycle of the appropriate IOT instruction.

Device Selector (DS)

The device selector, consisting of gates and pulse amplifiers, produces command pulses which set and clear registers and transfer information. The device selector primarily enables the memory extension control by combining the IOT and fetch levels with MB3 (0), MB4 (0) levels. The resulting MEM EXT level conditions various gates in the control circuits; the contents of bits 6 through 11 of the instruction word enable or disable these gates. This special gating is used in place of the normal type of device selector eliminating the pause feature of the IOT instructions and executing these instructions in 1.5 μsec.

MA Buffers

The MA buffers distribute the 1 and 0 levels from the MA flip-flops to the memory address selectors of fields 1 through 7. Each MA buffer consists of a bus driver capable of driving a 40-ma load.

Circuit Operations

The logic circuits of the Type 183 Memory Extension Control appear on engineering drawings BS-D-183-0-2 and BS-D-183-0-3. Engineering drawing UML-E-8M-0-20 shows the location of the modules. The majority of the modules are in positions 1 through 5 of rows MC, MD, ME, and MF. The in/out connectors for the memory extension control are in positions ME30 through ME33 and MF33. Adding a memory extension control to a basic PDP-8 system activates the three INST FIELD keys, three DATA FIELD keys, and the associated indicators of the operator console. These keys load information into the IF and DF, respectively, when the operator presses the LOAD ADD key. The following paragraphs describe the functional elements of the memory extension control.

Instruction Field Register (IF)

The IF is a 3-bit register utilizing 1-1/2 Type S205 Dual Flip-Flop modules in locations MD1 and MD2. A 0 ⟶ PC5-11 pulse from the PC control element in the processor clears the register. This pulse enters the memory extension control at terminal MD35F and triggers the Type S603 Pulse Amplifier circuit JFH in module ME4. A positive FIELD ⟶ SAVE pulse appears at terminal ME4F to clear the IB, IF, and DF. The same pulse strobes the contents of the IF into bits 0 through 2 of the SF, and the 1's contents of the DF into bits 3 through 5 of the SF.

A load address operation initially loads the IF. If the operator presses the LOAD ADD key, it generates an SR ⟶ PC pulse in the processor during time state SP2. This positive pulse enters the memory extension control at terminal MD35D to strobe binary 1's from the INST FIELD switch register (IFSR) into the IF and to strobe binary 1's from the DATA FIELD switch register (DFSR) into the DF.

The 1 levels of bits IF0, IF1, and IF2 are at terminals D, E, and F, respectively, of in/out connector MA35. From this connector, the signals arrive at the IF indicator lamp drivers on the operator console. These 1 levels also condition the DCD set gates of bits SF0, SF1, and SF2 in the save field register. The 1 and 0 levels of all three IF bits reach the instruction decoder module at location MC5.

Data Field Register (DF)

The DF is a 3-bit register utilizing three Type 201 Flip-Flops located in modules MD3 through MD5. Clearing and initial loading conditions for the DF and conditions for the transfer of binary 1's from the DF into the SF are identical to the corresponding conditions for the IF. During a CDF instruction, the contents of bits MB6 through MB8 jam-transfer into the DF. The Type S603 Pulse Amplifier circuit DFH in module MF17 generates the command pulse which performs this transfer. The NAND, combining the EXT GO enabling signal from the device selector with the MB11 (1) level, conditions the DCD input gate of this pulse amplifier. Timing pulse T2A and the MEM EXT level produce the EXT GO pulse in pulse amplifier LMN of the S603 module at ME4.

During an RMF instruction, the contents of save field register bits SF3 through SF5 jam-transfer into the DF in time state T2. The Type S603 Pulse Amplifier circuit KMN in module ME5 generates the command pulse which performs this transfer. The DCD input gate of this pulse amplifier is conditioned by the MB11 (1) level and is triggered by the EXT GO pulse from the device selector. This same pulse also jam-transfers the contents of bits SF0 through SF2 into the instruction buffer register.

The 1 levels of bits DF0, DF1, and DF2 are available at terminals K, M, and P, respectively, of in/out connector ME30, and at terminals A, B, and C of the connector at MA35. From connector MA35, the signals flow to the DF indicator lamps on the operator console. The 1 and 0 levels of all three DF bits reach the data decoder module at location MC4.

Instruction Buffer Register (IB)

The IB is a 3-bit register utilizing three Type R201 Flip-Flops located in modules ME1 through ME3. Clearing and initial loading conditions for the IB are identical to the corresponding conditions for the IF. Conditions for a jam-transfer from save field register bits SF0 through SF2 are identical to the conditions for a jam-transfer from bits SF3 through SF5 into the DF.

The contents of the IB jam-transfer into the IF during the fetch cycle of a directly addressed JMP or JMS instruction and also during the defer cycle of an indirectly addressed JMP or JMS instruction. The Type S603 Pulse Amplifier circuit TUV in module ME4 generates the command pulse which performs these transfers. During the fetch cycle of a directly addressed JMP or JMS instruction, an MB ⟶ PC0-4 ENABLE level generates in the PC control and enters the memory extension control at terminal R of in/out connector MD35. This level conditions the DCD input gate of the pulse amplifier, and timing pulse T1 triggers the gate and pulse amplifier. During the defer cycle of an indirectly addressed JMP or JMS instruction, an MB ⟶ PC5-11 ENABLE level generates in the PC control. This level enters the memory extension control at terminal E of in/out connector MD35 and inverts in the Type S107 inverter circuit NP of module ME8. The inverted level conditions the Type S111 Diode Gate circuit KLN in module ME6; timing pulse T1 triggers the gate. The output of the gate triggers the pulse amplifier which effects the IB ⟶ IF transfer.

During a CIF instruction, the contents of bits MB6 through MB8 jam-transfer into the IB to determine the memory field to be selected by the next JMP or JMS instruction. The Type S603 Pulse Amplifier circuit RTU in module ME5 generates the MB ⟶ IB command pulse which effects the transfer. Enabling signal MB10 (1) level conditions the DCD input gate of this pulse amplifier which is triggered by the EXT GO pulse.

Save Field Register (SF)

The SF is a 6-bit register utilizing two Type S203 Triple Flip-Flop modules at location MC1 and MC2. A 0 ⟶ SAVE command pulse generated by the Type S603 Pulse Amplifier circuit DFH in module ME4 clears the SF. The positive-going change in the output of a NAND gate that combines the INT ACK negative level from the program interrupt synchronization element of the processor with the F level from the major state generator, triggers and permanently conditions the DCD input gate of this pulse amplifier. The two triggering signals enter the memory extension control at terminals MD35B and MF36A, respectively. They trigger the pulse amplifier DCD gate during the fetch cycle of the JMS instruction forced by the granting of an interrupt. Under these conditions, timing pulse T2B causes the PC control to generate a 0 ⟶ PC5-11 pulse which enters the memory extension control at terminal MD35F. This pulse triggers pulse amplifier JFH in module ME5 to generate a FIELD ⟶ SAVE pulse. The FIELD ⟶ SAVE pulse transfers binary 1's from the IF and DF into the SF and clears the IF, DF, and IB.

Device Selector

The device selector consists of a 5-input NAND gate and an inverter. The diode input terminals of the NAND gate are terminals D and E of the Type S111 Diode Gate at location ME7, and terminals D, E,

and H of the Type R002 Diode Network at location MF4. The NAND gate combines the F level from the major state generator and the IOT level from the instruction register decoder with the MB3 (0), MB4 (1), and MB5 (0) levels. When all these levels are present, the gate gives an output, and the negative MEM EXT enabling level becomes available at inverter output terminal ME8L. This signal indicates that the current instruction is of the 6200 (memory extension IOT) class. Terminal ME8L goes to -3v, and a ground level $\overline{\text{MEM EXT}}$ level appears at inverter input terminal ME8M. The $\overline{\text{MEM EXT}}$ level inhibits generation of the 1 ⟶ PAUSE pulse. Therefore, execution of IOT instructions in this group takes the normal cycle time of 1.5 μsec, rather than the expanded 3.75 μsec time required for most IOT instructions. The MEM EXT level is the input to gating circuits which decode MB bits 7 through 9, to produce command pulses for the RDF, RIF, and RIB instructions at pulse amplifier output terminals MF5H, MF5N, and MF5U, respectively.

Field Decoders and Enable Field Signal Generator

The enable field signal generator consists of three Type S151 Binary-to-Octal Decoder modules at locations MC3, MC4, and MC5. Each of these decoder modules accepts three complementary pairs of input levels and produces one of eight possible ground levels determined by the bit combination. When the enable input at -3v, all the output lines are driven to -3v. When the enable input is at ground, only one of the output lines is at ground; the other seven remain at -3v.

The break decoder at location MC3 receives ADDRESS EXTEND signals from a high-speed I/O device using the data break facility, and the complements of these signals. The three inverters DE, FH, and JK in S107 module ME8 convert the three address lines to the three complementary lines required by the decoder.

The data decoder at location MC4 receives the three complementary signal levels from the DF. This decoder determines the field to be enabled for the retrieval of operands.

The instruction decoder at location MC5 receives the three complementary signal levels from the IF. This decoder determines the field to be enabled for the retrieval of instructions.

The break decoder enables only when the processor is in the break state. The B SET signal from the processor, which is double buffered by inverters DE and FH of the S107 module at ME7, performs enabling.

The data decoder enables only when the processor enters the execute state. A 2-input negative NAND gate DEH of the S111 Diode Gate module at MF1 determines this condition. The gate enables the data decoder when the $\overline{\text{JMP + JMS}}$ level and the D level (defer state) signals arrive from the processor.

The instruction decoder enables unless the break decoder is enabled, the data decoder is enabled or the processor is in the word count (WC) state. A 3-input diode-transistor gate enables the instruction decoder unless one of the following conditions exist:

1. The $\overline{\text{B SET}}$ level is at ground potential, indicating that the processor is in the break state thus enabling the break decoder.

2. The enabling level input to the data decoder is at ground potential, indicating that the next cycle will be an execute state requiring access to data in memory.

3. The WC + WC SET level is at ground potential, indicating that the WC cycle of a 3-cycle data break is in progress. This signal forces an ENABLE FIELD 0 signal since the CA and WC addresses used for this type of break must be in field 0.

The ENABLE FIELD lines 0 through 7 are normally held at -3v. However, a ground level from any one of the decoders overrides the negative level and enables the corresponding start field gate.

Start Field Gating

The start field gates and pulse amplifiers are in three Type S603 Pulse Amplifier modules at locations MA32, MA33, and MA34 (drawing BS-D-183-0-2). Each module contains three pulse amplifiers provided with DCD input gates. Eight of the nine pulse amplifiers generate a START FIELD pulse; the ninth accepts a positive timing pulse T1 from the processor timing circuits and generates a positive BT1 pulse which arrives at the memory fields to initiate the write cycle.

One of the eight possible ENABLE FIELD levels from the decoders of the enable field signal generator conditions each DCD gate. Only one of these levels appears at any one time. The MEM START signal from the processor timing circuits arrives at all of the DCD gates simultaneously and triggers the one conditioned by a ground ENABLE FIELD level. The associated pulse amplifier triggers and generates a START FIELD pulse to the selected memory field. There the pulse sets the MEM ENABLE flip-flop and starts the read cycle. The START FIELD 0 pulse starts the standard memory field which is part of the basic PDP-8 system. The START FIELD 1 through START FIELD 7 pulses are available on terminals D, E, H, K, M, P, and S of the in/out connector at location ME33.

MA Buffers

The buffers that supply address information to each field of extended memory from the MA appear in engineering drawing BS-D-183-0-2. These buffers consist of 12 Type B684 Bus Driver modules in locations

MB32 through MB35, MC32 through MC35, and MD32 through MD35. The direct output of each noninverting bus driver connects to terminals of connector ME32 or MF32 for distribution to all of the extended fields in parallel.

Interrupt Inhibit

The INT INHIBIT flip-flop disables the program interrupt synchronization element of the processor for the time between execution of a CIF instruction that sets up an instruction field and execution of either a JMP or JMS instruction that establishes the instruction field. This flip-flop is half of the S203 module at MD2. The negative output from this flip-flop, when in the 1 state, disables the circuits in the devices. The MB ⟶ IB pulse produced at execution of a CIF instruction sets the flip-flop and the IB ⟶ IF pulse (produced when the instruction field is entered by executing a JMP or JMS instruction) clears it.

Accumulator Transfer Gating

The accumulator gates consist of two Type R123 Diode Gate modules and one Type S111 Diode Gate module. Each gate has two inputs: a register 1 output level conditions one; a command pulse triggers the other. The gating circuits produce six positive output pulses, IM6 through IM11. These pulses arrive at the direct set inputs of flip-flops AC6 through AC11 in the accumulator register of the processor. They leave the memory extension control from terminals J, K, L, M, and P of the connector at location MD35 and enter the processor on the same terminals of the normal interface connector at location PD2.

During an RIB instruction, the MB7(1), MB8 (1), and MB9 (1) levels condition the diode gate inputs L, M, and P in module MF2; these levels combine with the MEM EXT enabling level, applied at terminal MF3S. When timing pulse T1 occurs, the gate triggers pulse amplifier RUV of the Type 640 at location MF5 to produce an SF ⟶ AC command pulse. The accumulator gates strobe the contents of the SF into bits 6 through 11 of the AC.

During an RIF instruction the MEM EXT, MB7 (1), MB8 (0), and MB9 (1) levels trigger the Type S111 Diode Gate in module MF3. When timing pulse T1 occurs, the gate triggers the Type W640 Pulse Amplifier circuit KNP in module MF5 to produce an IF ⟶ AC command pulse. The accumulator gating strobes the contents of the IF into bits 6 through 8 of the AC.

During an RDF instruction, the MEM EXT, MB7 (0), MB8 (1), and MB9 (1) levels condition the Type S111 Diode Gate in module MF3. When timing pulse T1 occurs, the gate triggers the Type W640 Pulse Amplifier circuit DHJ in module MF5 to produce a DF ⟶ AC command pulse. The accumulator gating strobes the contents of the DF into bits 6 through 8 of the AC.

TYPE 184 MEMORY MODULE

To extend PDP-8 core memory beyond the standard 4096-word capacity, add Type 184 Memory Modules to the system. Up to seven memory modules, each containing a field of 4096 words, can be added to a standard PDP-8, increasing the storage capacity of the system to a maximum of 32,768 words. Addition of from one to seven memory modules requires the use of a Type 183 Memory Extension Control.

Each Type 184 Memory Module consists of a core array, address selection circuits, inhibit selection circuits, sense amplifiers, a master slice control, and memory control circuits identical to those employed in the standard PDP-8 core memory. The minor differences are chiefly in the input signals. The memory selectors do not receive address signals directly from the processor MA, but from bus drivers in the memory extension control. These bus drivers receive MA (1) and (0) levels from the processor MA. The memory control circuits do not receive a MEM START signal from the processor timing circuits; instead, memory modules used for extension receive a START FIELD pulse from the start field gating circuits of the memory extension control. A given field of an extended memory receives a START FIELD pulse only when that field is selected by the memory extension control.

TYPE 188 MEMORY PARITY OPTION

The Type 188 Memory Parity option provides a data transmission check of each word written into or retrieved from memory. A parity bit generator samples the contents of each bit of the MB and generates a 13th (parity) bit which is written into memory in a 13th plane so that the entire word contains an odd number of binary 1's. During the read operation, binary 1's in twelve of the memory planes set the corresponding flip-flops of the MB; a binary 1 in the parity plane sets the PARITY flip-flop in the parity option. In sampling the contents of all 13 flip-flops, if an even number of binary 1's is found, a parity error signal generates to set the PARITY ERROR flag. This flag connects to the program interrupt synchronization element of the processor to initiate a program interrupt.

Logical Functions

Two IOT instructions can occur with the memory parity option. The Skip on No Memory Parity Error (SMP) instruction has the octal code 6101 and causes sensing of the PARITY ERROR flag. If this flip-flop contains a 0, the contents of the PC increment by 1 at event time 1, skipping the next instruction. If the PARITY ERROR flip-flop contains a 1, the next instruction occurs and initiates an appropriate subroutine. The Clear Memory Parity Error Flag (CMP) instruction has the octal code 6104, and the PARITY ERROR flag clears at event time 3. When a parity error occurs, the PARITY ERROR flag sets, initiating a program interrupt subroutine. The SMP instruction, executed in the interrupt subroutine, samples the condition of the PARITY ERROR flip-flop to determine the cause of the interrupt.

Circuit Operations

The logic of the Type 188 Memory Parity option appears in engineering drawing BS-D-188-0-2. The option consists of two major functional elements: the parity network and the control circuits.

Parity Network

The parity network monitors the contents of the MB during a write operation and generates a 0 for the core memory parity bit if the MB contains an odd number of binary 1's. The network monitors the contents of the MB and of the PARITY flip-flop during a read operation and generates a parity error signal if the combined contents contain an even number of binary 1's.

The parity network consists of six Type B130 Three-Bit Parity modules, at locations ME11 through ME14, MF12, and MF13. The four modules at locations ME11 through ME14 monitor the contents of the MB in groups of three bits. Each module consists of four 3-input negative AND gates feeding a 4-input OR gate. Three of the AND gates detect a binary 1 in the most significant, middle, or least significant bit of the group, respectively. The fourth AND gate gives an output only if all three bits contain 1's. The parity module produces a negative level at terminal D if the bit group contains either one or three binary 1's. A negative level appears at terminal E if the bit group contains two binary 1's.

The parity module at location MF12 combines the outputs of the modules at locations ME11, ME12, and ME13, which monitor bits MB0 through MB8. The parity module at location MF13 combines the outputs of modules MF12, ME14 (monitoring bits MB9 through MB11), and the PARITY flip-flop. During a write operation, the PARITY flip-flop clears T1. If bits MB0 through MB11 contain an even number of binary 1's, a ground level PARITY = 0 level appears at terminal MF13D and is applied to the parity bit inhibit driver so that a 1 writes into the parity plane of core memory. If bits MB0 through MB11 contain an odd number of binary 1's, a negative level appears at terminal MF13D and inhibits the selected core of the parity plane so that a binary 0 is written. The output level of the PARITY flip-flop is ignored, since it is always 0 during a write operation.

During a read operation, the MEMORY START pulse clears the PARITY flip-flop; and when the strobe occurs, the sense amplifier associated with the parity plane sets the PARITY flip-flop to 1 if the plane contains a 1. If the plane contains a 0, the sense amplifier gives no output and the PARITY flip-flop remains at 0. The negative PARITY = 0 level may appear at terminal MF13D under either of the following conditions:

1. If the PARITY flip-flop contains a 0 and bits MB0 through MB11 contain an odd number of binary 2's

2. If the PARITY flip-flop contains a 1 and bits MB0 through MB11 contain an even number of binary 1's

Any other condition constitutes a parity error and causes a ground level to appear at terminal MF13D and a negative parity error level to appear at terminal MF13E.

Control Circuits

There are three control circuits: a flag-setting circuit, a flag-clearing circuit, and a skip circuit.

The flag-setting circuit includes the PARITY ERROR flip-flop, a delay network, and gates and inverters. The MEM STROBE signal from the memory control arrives at the input terminal MF9E of an inverter, and the output of the inverter triggers a pulse amplifier in the Type B360 Delay With Pulse Amplifier module at MF8. The output pulse of the pulse amplifier, delayed long enough to permit the MB and PARITY flip-flops to be set by the sense amplifiers, samples the parity error signal. This sampling occurs in a 2-inverter gate composed of the output buffer of the B360 module and inverter JKL of the B104 module at location MF9. If the parity error signal from the parity network is negative (indicating a parity error condition) when the reshaped and delayed MEM STROBE pulse occurs, pulse amplifier TUT of the module at MF10 sets the PARITY ERROR flip-flop (flag). The PARITY ERROR (1) level is buffer inverted in module ME10 and appears as an INTERRUPT BUS IN ground level signal at terminal ME10U. This terminal connects to the normal interface terminal for an interrupt request.

The flag-clearing circuit serves as a device selector for the CMP instruction and consists of a 6-input diode gate and a pulse amplifier. In the CMP instruction (6104_8), bits MB3, MB4, MB6, MB7, and MB8 all contain a 0 and bit MB5 contains a 1. These assertion levels NAND combine in modules ME9 and ME10 to condition the DCD level input terminal MF10L of the associated pulse amplifier. During the pause period, since bit MB11 is also a 1, pulse IOP4 generates at event time 3 and triggers the pulse amplifier. A positive CMP pulse appears at terminal MF10M and clears the PARITY ERROR flip-flop.

The skip control circuit, consisting of a 7-input diode gate and a pulse amplifier, serves as a device selector for the SMP instruction. In the SMP instruction (6101_8), bits MB3, MB4, MB6, MB7, and MB8 are 0 and MB5 is 1. These assertion levels NAND combine with the PARITY ERROR (0) level to condition the DCD input level terminal MF10E of the associated pulse amplifier. Since bit MB11 is also a 1, pulse IOP1 generates during the pause period and triggers the pulse amplifier. A COUNT PC pulse appears at terminal

MF10F, and increments by 1 the contents of the PC. The computer then skips the next instruction. If the PARITY ERROR flip-flop is set to 1, the conditions for the skip are not met, and the DCD gate remains inhibited. Therefore, the next instruction occurs (usually initiating a subroutine to determine the cause of the parity error).

CHAPTER 5

INPUT/OUTPUT

Signals which pass between peripheral equipment and the PDP-8 are usually pulses supplied to a processor input bus, or static levels supplied as processor output signals which may be sampled or strobed by a selected I/O device. Exceptions to this rule are the address and data signals which arrive at the processor during data break operations as static levels, and the WC OVERFLOW, ADDRESS ACCEPTED, and IOP pulses, which are pulse outputs of the processor. The bussed nature of input/output signals of the processor requires that the peripheral equipment contain gating circuits to control the application of input pulses to the processor and timing control circuits to strobe processor output lines to transfer information into external device buffers. The design of circuits which perform these operations in input/output equipment depends upon the characteristics of the processor interface circuits as described in Chapter 6, the functional operation of the processor interface logic elements as explained in Chapter 3, and by the nature of the circuits in the peripheral equipment which receives or transmits signals. Gating circuits in peripheral equipment that supply input pulses to the processor are similar to those on the processor drawings for standard input/output devices.

Programmed information transfers (including initializing of equipment using the data break facility) between the processor and all other devices require that a preestablished select code in bits 3 through 8 of an IOT instruction enable each circuit (or group of circuits) transmitting or receiving information, and that transfers synchronize with the processor timing. A NAND gate and pulse amplifier circuits, serving as a device selector, perform these operations. Typical device selectors appear in engineering drawing 10 for the program interrupt synchronization element and on engineering drawing 11 for the Teletype control. An outline of a device selector suitable for peripheral equipment is at the end of this chapter.

The standard peripheral equipment supplied with a PDP-8 consists of a Teletype Model 33 Automatic Send Receive Set and a Teletype Control, which are described in this chapter. Except for the Type 189 Analog-to-Digital Converter, described in this chapter because it is intricately involved in the operations of the PDP-8 and wired into the system (adding this option to the computer requires little more than the insertion of the modules into the module connector blocks), other optional peripheral equipment is described in separate documents. The Type KR01 Automatic Restart, Type 182 Extended Arithmetic Element, and Type 681 Data Line Interface options described in Chapter 3 of this manual and the Type 183 Memory Extension Control, Type 184 Memory Module, and Type 188 Memory Parity options described in Chapter 4 of this manual are not peripheral equipment since these options are integral parts of the system and functionally inseparable from the processor.

TELETYPE MODEL 33 AUTOMATIC SEND RECEIVE SET

The Teletype unit supplied as standard equipment with a PDP-8 serves as a keyboard input and page printer output, and as a perforated-tape reader input and a tape-punch output device. This unit is a standard Model 33 Automatic Send and Receive Set (ASR) as described in Teletype Corporation bulletins 273B and 1184B. For operation with the PDP-8, this unit is modified as follows:

1. The WRU (who are you) pawl is removed. This pawl is used only when several Teletypes connect in a communication system so that a unit receiving a message sends a "who are you" message to the transmitting unit which automatically produces the "here is" identification code and supplies it to the receiving station. In the computer system this pawl is removed to prevent insertion of the "here is" code into data supplied to the computer from the Teletype unit.

2. Cables are connected between the Teletype unit and the control as appears in engineering drawing 11. Signal cables connect to a terminal block within the stand. A relay is added and connections are made to the tape reader advance magnet. These connections enable tape motion while the control assembles a character, and disable the magnet when the keyboard flag is a 1, indicating that the assembled character is ready for transfer to the computer.

This modification takes only a few minutes and does not permanently limit any normal use of the 33 ASR.

TELETYPE CONTROL (18)

The control assembles or disassembles serial information for the Teletype unit for parallel transfer to or from the accumulator of the processor. The control also provides the flags which cause a program interrupt or an instruction skip based upon the availability of the Teletype unit, thus controlling the rate of information transfer flow between the Teletype and the processor as a function of the program. Engineering drawing 11 shows the control and interface connections between the control and the Teletype unit. Table 5-1 indicates interface connections between the control and the processor.

In all programmed operation, the Teletype unit is considered two separate devices: a Teletype input device (TTI) from the keyboard or the perforated-tape reader; and a Teletype output device (TTO) for computer output information to be printed and/or punched on tape. Therefore, two device selectors are used, consisting of 6-input NAND gates at locations ME17 and ME18 (11, A2 and B1). One of these is assigned the select code of 03 to initiate operations associated with the keyboard/reader, and the other is assigned the select code of 04 to perform operations associated with the teleprinter/punch. Corresponding IOT

TABLE 5-1 TELETYPE CONTROL INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction*	Teletype Control Terminal
	Logic Element	Engineering Drawing	Terminal		
PWR CLR	Power Clear Generator	9	PD33U	⟶▷	MF36M
BAC4 (1)	AC	16	MF34M	⟶◇	ME22S
BAC5 (1)	AC	16	MF34P	⟶◇	ME23P
BAC6 (1)	AC	16	MF34S	⟶◇	ME23R
BAC7 (1)	AC	16	MF34T	⟶◇	ME23S
BAC8 (1)	AC	16	ME34V	⟶◇	ME24P
BAC9 (1)	AC	16	MF34D	⟶◇	ME24R
BAC10 (1)	AC	16	MF34E	⟶◇	ME24S
BAC11 (1)	AC	16		⟶◇	ME25H
INTERRUPT BUS IN	Interrupt Sync	10	PF1S	◁⟵	MF36S
COUNT PC	PC Control	11	PF1R	◁⟵	MF36R
TTI ⟶ AC	AC	2	PF1P	◁⟵	MF36P
KCC IOT 032	AC Control	3	PF1U	◁⟵	MF36U
IOP1	IOP Generator	10	PF1J	⟶▷	MF36J
IOP2	IOP Generator	10	PF1K	⟶▷	MF36K
IOP4	IOP Generator	10	PF1L	⟶▷	MF36L
MB3-4 (0)	MB	5	PD1R,T	⟶◆	MD36R,T
MB5-8 (0)	MB	5	PE1D,F,J,L	⟶◆	ME36D,F,J,L
MB7-8 (1)	MB	5	PE1K,M	⟶◆	ME36K,M
TTI0 (0)	AC	2	PB1A	◇⟵	MB36A
TTI1 (0)	AC	2	PB1B	◇⟵	MB36B
TTI2 (0)	AC	2	PC1A	◇⟵	MC36A
TTI3 (0)	AC	2	PC1B	◇⟵	MC36B
TTI4 (0)	AC	2	PD1A	◇⟵	MD36A
TTI5 (0)	AC	2	PD1B	◇⟵	MD36B
TTI6 (0)	AC	2	PE1A	◇⟵	ME36A
TTI7 (0)	AC	2	PE1B	◇⟵	MF36B

*Arrows pointing right designate processor output; arrows pointing left designate processor inputs.

pulses from the two device selectors perform parallel input and output functions. Pulses from the IOP1 pulse trigger the skip control element; pulses from the IOP2 pulse clear the control flags and/or the accumulator; and pulses produced by the IOP4 pulse initiate data transfers to or from the control.

Signals used by the Teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current) and spaces (no current). Each 11-unit Teletype character consists of a 1-unit start space, eight 1-unit character bits, and a 2-unit stop mark. The 8-bit flip-flop TTI shift register at locations MF22 through MF24 receive the Teletype characters from the keyboard/reader. The character code of a Teletype character loads into the TTI so that spaces correspond with binary 1's and marks correspond to binary 0's. Upon program command the complement of the contents of the TTI transfers in parallel to the accumulator. Eight-bit computer characters from the accumulator load in parallel into the 8-bit flip-flop shift register TTO at locations ME22 through ME25 for transmission to the Teletype unit. The TTO clock generates the start space, then shifts the eight character bits into a flip-flop which controls the printer selector magnets of the Teletype unit, and then produces the stop mark. This transfer of information from the TTO into the Teletype unit occurs in serial manner at the normal Teletype rate.

A ground IN ACTIVE signal flows from the control circuit of the Teletype incoming line unit module when a Teletype character starts to enter the TTI. This signal clears the READER RUN flip-flop, which in turn energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed and before sensing of the next character begins. The KEYBOARD FLAG flip-flop sets and causes a program interrupt when an 8-bit computer character has been assembled in the TTI from a Teletype character. The program senses the condition of this flag with a KSF microinstruction (skip if keyboard flag is a 1, IOT 6031) and issues a KRB microinstruction (IOT 6036) which clears the AC, clears the keyboard flag, transfers the contents of the TTI into the AC, and sets the READER RUN flip-flop to enable advance of the tape feed mechanism.

A TELEPRINTER FLG flip-flop sets when the last bit of the Teletype code has been sent to the teleprinter/punch, indicating that the TTO is ready to receive a new character from the AC. This flag connects to both the program interrupt synchronization element and the skip control element. Upon detecting the set set condition of the flag by the TSF microinstruction (skip if teleprinter flag is a 1, IOT 6041), the program issues a TLS microinstruction (IOT 6046) which clears the flag and loads a new computer character into the TTO.

Operation of the Teletype incoming line unit TTI requires an input clock signal which is eight times the baud frequency of the Teletype unit. This signal controls the strobing of Teletype information into the TTI during the center of each baud (which is the most reliable time for sensing) and controls the shifting of information through the flip-flops of the TTI. The Teletype transmitter requires an input clock frequency

which is the same as the baud frequency of the Teletype unit. This signal controls the shifting of the TTO and thus determines the timing of the 11-unit-code Teletype character it generates. The three Type S202 Dual Flip-Flops at locations MF14 through MF16 produce the TTI CLOCK and TTO CLOCK signals. These six flip-flops form a binary counter which provides frequency division of the output from the Type R405 Crystal Clock module at location ME15. This frequency division method is used since electronic clocks are not reliable at the low frequency required for Teletype operation. The 7.04-kc frequency of the clock is 64 times the baud frequency of the Teletype unit. Division of the clock frequency by 8 (three binary flip-flops) yields the TTI CLOCK signal, which is eight times the baud frequency, and division by 64 (six binary flip-flops) yields the TTO CLOCK signal, which corresponds with the baud frequency.

TYPE 189 ANALOG-TO-DIGITAL CONVERTER (189-0-2)

The Type 189 Converter operates in the conventional successive-approximation manner, using the memory buffer register as a distributor shift register and using the accumulator as the digital buffer register. The converter logic consists of some timing and control circuits, a 12-bit digital-to-analog converter, and a comparator. An ADC instruction, which produces a pause and clears the accumulator, initiates converter operation. The conversion process starts by assuming that the value of the analog input signal is at mid-scale. A binary 1 is therefore set into the most significant bit of the MB and transfers to accumulator bit AC0. This causes the digital-to-analog converter, whose output is a function of the number contained in the AC, to produce a voltage equal to the center of the converter range (ground to −10v). The output of the D/A converter, representing the first approximation of the input signal, is then compared with the actual analog input signal. If the approximated voltage is greater than the analog signal voltage, the AC bit clears. The binary 1 in bit MB0 then shifts one place to the right and transfers into the corresponding bit of the AC. The number in the AC is 4000 if the approximated voltage was less than the analog input signal or is 6000 if the approximated voltage was greater than the analog input during the previous step. The new number in the AC causes the D/A converter to generate a new approximated voltage. If this voltage is still too large, the clear and shift right process repeats, and the binary 1 now appears in bit AC2. The approximated voltage is again compared with the analog input signal. Each successive approximation reduces by one half the difference (error) between the value of the analog input signal and the value of its digital representation in the AC.

The location of the binary 1 in the MB controls the number of approximations made, and hence the accuracy of the conversion. Since the conversion starts when the binary 1 shifts right, one conversion takes place after sensing of the MB bit which discontinues the conversion process. At the conclusion of the conversion, the unsigned binary number in the accumulator is accurate to one half of the digital value

of the least significant bit sensed. At the conclusion of the conversion process the converter produces a RESTART SYNC (1) pulse. This pulse causes the computer program to continue, and the restart process automatically clears the MB.

The Type 189 Analog-to-Digital Converter is completely wired in the standard PDP-8, so that addition of the option requires only the insertion of modules into their connector blocks, installation of an input signal cable terminated with a BNC connector, and presetting of the conversion accuracy. The converter is composed of modules at locations PE5, PE11 through PE16, and PF11 through PF16. The block schematic for the logic circuits is engineering drawing BS-D-189-0-2, and interface connections between the converter and the processor appear in Table 5-2. Note that the input connections to converter terminal PE12J is one of six possible connections to the MB, and the connection used determines the accuracy of the conversion. Table 5-3 indicates the MB terminals which may be used for this connection, and lists other characteristics of the converter which the accuracy connection affects. To save program running time, the converter should be preset to provide only the accuracy required by the program application. Maximum error of the converter is equal to the switching point error plus the quantization error. Maximum quantization error is equal to plus or minus one half of the digital value of the least significant bit. Table 5-3 also indicates switching point error, total conversion time, and execution time of the IOT instruction which initiates operation of the converter.

TABLE 5-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction*	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
AC0 (1)	AC	2	PA7AP	——◇	PF11U
AC1 (1)	AC	2	PA8AP	——◇	PF11T
AC2 (1)	AC	2	PA9AP	——◇	PF12U
AC3 (1)	AC	2	PA10AP	——◇	PF12T
AC4 (1)	AC	2	PA11AP	——◇	PF13U
AC5 (1)	AC	2	PA12AP	——◇	PF13T
AC6 (1)	AC	2	PA13AP	——◇	PF14U
AC7 (1)	AC	2	PA14AP	——◇	PF14T
AC8 (1)	AC	2	PA15AP	——◇	PF14V
AC9 (1)	AC	2	PA16AP	——◇	PF15U

*Arrows pointing right designate converter input signals; arrows pointing left designate converter output signals.

TABLE 5-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR (continued)

Signal	Processor			Symbol and Direction*	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
AC10 (1)	AC	2	PA17AP	——◇	PF15T
AC11 (1)	AC	2	PA18AP	——◇	PF15V
IOT 00	Processor Device IOT Selector	10	PC23T	——▷	PE15R
T1	Timing	9	PB33L	——▶	PA27R
PROCESSOR IOT	Processor Device IOT Selector	10	PB33T	——◆	PD34T
MB9 (1)	MB	5	PC16CD	——◇	PE15S
MB9 (1)	MB	5	PC16CF	——◆	PA27S
A/D CONV	AC	2	PA7BP thru PA18BP	◁——	PE10V
SHIFT MB	MB	5	PC7DU thru PC18DU	◁——	PE15F
RESTART SYNC	Program Sync	10	PC32S	◁——	PE15M
$\overline{\text{RUN STOP}}$	Run Control	9	PB33D	——◇	PE15L
IOT 004	AC Control	3	PA26L	◁——	PE15T
COMPARATOR	AC	2	PA7BV thru PA18BV	◇——	PD26T
A/D START (1)	AC	2	PA7BU	◇——	PE12L
A/D START (1)	MB	5	PC7DP	◇——	PE12L
A/D START (0)	MB	5	PC7DR	◇——	PE12M
PAUSE (1)	Pause Control	10	PC32L	◁——	PA27U

*Arrows pointing right designate converter input signals; arrows pointing left designate converter output signals.

An ADC instruction having the code 6004 initiates operation of the converter. The 0's contained in bits MB3 through MB8 of this instruction cause the processor IOT device selector (00) to produce a negative PROCESSOR IOT level at terminal PB33T and a positive IOT 00 pulse at terminal PC23T. In the converter, the PROCESSOR IOT level combines with an MB9 (1) level and a T1 pulse to produce a PAUSE (1) pulse at device selector output terminal PA27U. This pulse sets the PAUSE flip-flop to 1, thereby halting the computer program without initiating operation of the IOP pulse generator. In the converter an IOT 00 pulse triggers DCD input gate RS of module PE15 when the gate is enabled by the ground MB9 (1) level.

The output of the gate triggers the associated pulse amplifier to produce an IOT 004 pulse at terminal PE15T. The IOT 004 pulse performs the following operations:

1. In the AC control the IOT 004 pulse causes generation of a ⟶ AC pulse that clears the AC.

2. In the converter, the IOT 004 pulse sets the A/D ENABLE flip-flop via the direct-set input, and sets the A/D START flip-flop via the DCD gate input.

TABLE 5-3 ANALOG-TO-DIGITAL CONVERTER TYPE 189 CHARACTERISTICS

Adjusted Bit Accuracy	Origin of MB Signal of PE12J	Switching Point Error (percent)	Conversion Time per Bit (in μsec)	Total Conversion Time (in μsec)	Instruction Execution Time (in μsec)
6	PC12CF	±1.6	1.0	6	7.6
7	PC13CF	±0.8	1.85	13	14.6
8	PC14CF	±0.4	2.5	20	21.6
9	PC15CF	±0.2	2.7	24	25.6
10	PC16CF	±0.1	2.7	27	28.6
11	PC17CF	±0.05	4.1	45	46.6
12	PC18CF	±0.025	4.6	55	56.6

The A/D ENABLE flip-flop controls the length of time the converter operates. When the ADC instruction is issued, this flip-flop is set to 1 and remains in this state until the 1 in the MB has reached the desired (prewired) conversion bit accuracy. During the next to last conversion the A/D CONV pulse clears the A/D ENABLE flip-flop, thereby disabling the converter at completion of the next conversion.

The ground A/D ENABLE (1) level conditions the DCD input gate of the Type R302 Delay module at PE10. The negative A/D ENABLE (1) level enables the Type R401 Variable Clock module at PE13, which produces 100-nsec pulses to trigger the DCD gate of the delay one-shot. The one-shot gives an A/D CONV output pulse after a delay of 0.5 μsec.

Both the 1 and 0 outputs of the A/D START flip-flop flow to complementary gates of the R123 module at location PC5. The F(1) level from the major state generator enables these gates to produce the ground level MB0 SHIFT ENBL (0) and MB0 SHIFT ENBL (1) levels which set up the DCD gates to shift the 1 through the MB. The DCD gates of the MB for bits 1 through 11, conditioned by the state of the next greater significant bit flip-flop, respond to the SHIFT MB pulse to shift a 1 into the MB for the

first conversion, and to shift it through the MB until the desired accuracy is obtained. This gating of the outputs of the A/D START flip-flop occurs in circuits of the Type R123 module at location PE5 and appears in engineering drawing BS-D-681-0-2.

The binary 1 output of the A/D START flip-flop enables a DCD gate at the set-to-1 input of the most significant bit of the AC. A/D CONV signals trigger this DCD gate. The A/D CONV signal is the positive-going level transition produced at terminal PE10V when the one-shot reverts to its stable state.

The delay one-shot reverts to its stable state and produces A/D CONV and MB SHIFT signals; the next converter clock pulse triggers it again. Thus, the one-shot continues to produce A/D CONV and MB SHIFT signals for as long as the A/D ENABLE flip-flop is in the 1 state. (The MB SHIFT pulse generates when the Type 681 Data Line Interface option (see engineering drawing BS-D-681-0-2) triggers pulse amplifier DFHJ of the S603 module at PE15.)

When the MB accuracy control bit becomes a binary 1, the MBn (1) ground level conditions the DCD input gate of the A/D ENABLE flip-flop. The next A/D CONV transition triggers the gate and resets the A/D ENABLE flip-flop to 0, thereby disabling the clock and delay one-shot, and stopping the conversion process. The number stored in the accumulator is the digital equivalent of the analog input signal (within the specified accuracy).

The positive-going level transition, which occurs at terminal PE12E when the A/D ENABLE flip-flop clears, triggers pulse amplifier KIMN of module PE15, provided that a $\overline{\text{RUN STOP}}$ level from the processor run control circuits conditions the DCD gate. The pulse amplifier produces a RESTART SYNC (1) pulse, which sets the RESTART SYNC flip-flop of the pause control to 1. Then the computer program restarts, following the discussion of the run and pause control in Chapter 3 of this manual.

The accumulator, cleared by the IOT 6004 pulse and with a binary 1 set into its most significant bit, contains a binary number which corresponds to one half of its possible maximum value during the first approximation. Each bit of the accumulator supplies the input to a level amplifier of the modules at locations PF11 through PF15. The level amplifiers also receive a −10v potential from the output of the Type A704 −10v Precision Power Supply module at location PE16. Each level amplifier circuit provides an output ground potential when the input signal is at ground level (ACj (1)), and produces a −10v output signal when the input is at −3v (ACj (0)). The outputs from all level amplifiers combine in the digital-to-analog sections of the Type A601 and A604 modules. The analog voltage appearing at terminal PF11K represents the binary number contained in the AC. This voltage is compared with the analog input signal to be measured in the Type A502 Difference Amplifier module at location PE11. The output (at terminal F) of this difference amplifier is −3v if the input from the converter (at terminal P) is more negative than the analog

input signal (at terminal N) being measured. The output of this amplifier is at ground potential if the input from the converter is more positive than the analog input signal. This output is inverted and arrives at the AC as the COMPARATOR signal.

The COMPARATOR signal flows to one input of a 3-input ground-level DCD gate at the 0 input of each AC flip-flop. The corresponding bit of the memory buffer register in the 1 state enables the second input to each DCD gate. When the DCD gate is enabled by both conditions, the A/D CONV pulse triggers it to clear the AC flip-flop. The binary 1 state of the next more significant bit of the memory buffer register enables a corresponding positive DCD gate at the set-to-1 input of each AC flip-flop. The binary 1 state of the A/D START flip-flop of the converter conditions this input to the set-to-1 DCD gate of AC0. These DCD gates trigger at the conclusion of each delay period of the integrating single shot. At this time also, the SHIFT MB signal shifts the contents of the MB one position to the right. This shifting results from a jam-transfer of information from the next more significant bit of the MB (and from the A/D START flip-flop for MB0). This operation transfers a binary 1 into MB0 during the first conversion and shifts it to the right for each successive conversion. The MB bit containing a 1 enables the next less significant bit of the accumulator to be set to 1 for the next approximation.

In summary, the IOT 6004 pulse clears the MB and AC; establishes a pause; starts operation of a clock and a one-shot, whose period is determined by the time required to generate and compare an analog signal with the signal to be measured; and sets the A/D START flip-flop which serves as a one-bit extension of the MB. When the one-shot period elapses for the first time, the contents of the MB shift to the right so that all bits contain 0's except the most significant bit, which contains a 1. At this time also, the most significant bit of the AC is set to 1. The contents of the AC then produce an analog signal which is compared with the signal to be measured. If the generated analog signal is more negative (greater amplitude) than the signal being measured, the COMPARATOR signal is at ground level, enabling the DCD gate at the clear input of AC0. When the time period of the one-shot elapses again, AC0 clears if the COMPARATOR signal is at ground potential, and AC1 is set to 1 from the contents of MB0. This operation of setting a 1 into the next least significant AC flip-flop, producing a comparator signal to clear the AC bit, and advancing a binary 1 through MB, continues until the one-shot and clock are disabled by the resetting of the A/D ENABLE flip-flop. This occurs when the binary 1 shifted through the MB reaches a preselected bit. The A/D ENABLE (0) transition causes a pulse amplifier to produce the RESTART SYNC (1) signal, which restores the processor timing signal generator to allow the program to continue and clears the MB. At this time the AC holds an unsigned binary number that corresponds with the value of the analog input signal. This number can be processed under program control.

SPECIAL INPUT/OUTPUT DEVICE MODULES

Because all I/O devices and peripheral equipment connect to a common I/O bus system, each external unit must have a device selector capable of recognizing the device selection code assigned to that unit. In addition, the device selector must be able to accept the three IOP pulses and combine these with the device code to produce IOT pulses for equipment control. Further, since the I/O information lines are common to all equipment, each external unit that transfers information into or out of the accumulator must have suitable gates at the output and input of the data register. The Type W103 Device Selector module and the Type R123 Diode Gate module meet all the requirements of the PDP-8 I/O system and permit connection of a wide variety of devices into the system.

Type W103 Device Selector

This double-height FLIP CHIP module contains a 14-input diode gate, and additional gates and pulse amplifiers for the production of IOT pulses. Figure 5-1 shows the internal logic of the module.

Negative MB (1) and MB (0) assertion levels corresponding to bits 3 through 8 of the IOT instruction serve as the select code input to the device and are applied to the 14-input NAND gate via input terminals BE through BT. Terminals BU and BV are available for the connection of any other level that governs selection of the device. Input terminals not used should be left unconnected. If the 1 and 0 levels of bits MB3 through MB8 are all permanently wired to the connector block, diodes corresponding to the unasserted levels should be removed from the module.

When all the required levels are present at the input terminals, terminal BD is driven from −3v to ground. This ground level indicates selection of the device and may be used in the control logic of the device. The ground level appearing at terminal BD also enables three IOP input gates. The IOP 1, IOP 2, and IOP 4 pulses arrive at terminals AP, AK, and AR, respectively. Each of these gates, when conditioned by the device selection level and strobed by an IOP pulse, triggers an associated pulse amplifier. The pulse amplifiers are similar to the Type R601 Pulse Amplifier described in the FLIP CHIP catalog, C-105; for driving capabilities and other characteristics, refer to the catalog. Each pulse amplifier provides both positive and negative IOT output pulses; these may be either 100 nsec or 400 nsec in duration, depending upon the pulse amplifier timing connections.

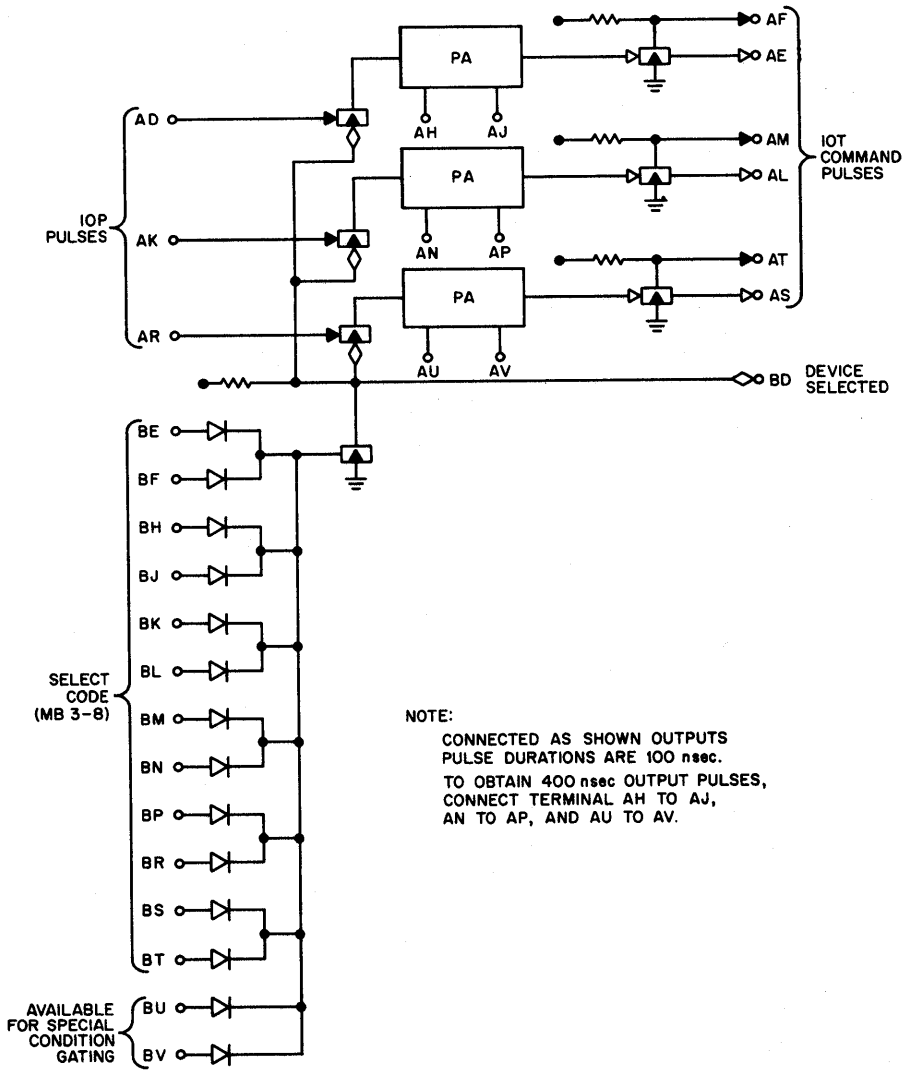
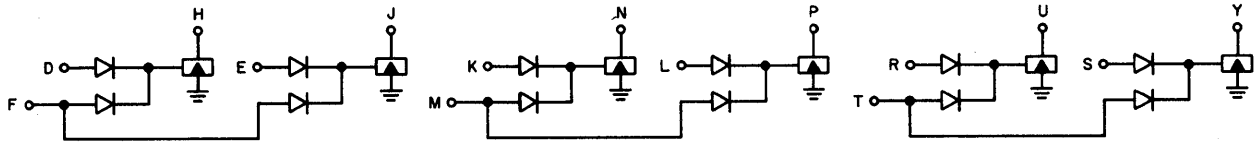


Figure 5-1 Type W103 Device Selector Module Logic Diagram

Type R123 Diode Gate

This standard FLIP CHIP module contains six 2-input negative NAND diode gates. Figure 5-2 shows the internal logic of the module. When used as an I/O device output gate, the conditioning levels from the output of the AC or data register should be applied to terminals D, E, K, L, R, and S; the IOT strobe pulse that opens the gates should be applied to terminals F, M, and T. In this manner, data register flip-flop outputs in the 1 state (−3v) cause the appropriate AC input bus to be driven to ground when a negative IOT pulse triggers the gate. Driving the input bus to ground sets a 1 into the corresponding AC flip-flop. In a similar manner the AC outputs in the 1 state cause the IOT pulse to produce a positive pulse which can be used to set the appropriate flip-flop of the data register.



NOTES:
1. STROBE PULSE INPUT TO TERMINALS F, M, AND T WHICH ARE CONNECTED IN COMMON WHEN USED AS A BUS GATE
2. DATA BIT INPUTS TO TERMINALS D, E, K, L, R, AND S
3. TWO MODULES ARE REQUIRED TO STROBE A 12-BIT WORD

Figure 5-2 Type R123 Diode Gate Module Logic Diagram

CHAPTER 6

INTERFACE

All interface connections to the PDP-8 are made at assigned module receptacle connectors at the back of the memory M or processor P module mounting frame. The module receptacles and assigned use for interface signal connections are:

Receptacle	Signal Use
PE2	AC 0-8 inputs
PE3	Data address 0-8 inputs
PE4	Data bit 0-8 inputs
PF2	AC 9-11, skip, clear AC inputs and run output
PF3	Data address 9-11 inputs, and address accepted and B break outputs
PF4	Data bit 9-11 inputs
ME30	Address extend 1, 2, 3 inputs and data field 0-2 outputs
ME34	BAC 0-8 outputs
ME35	BMB 0-5 outputs
MF34	BAC 9-11, IOPs, BT1, BT2A, and power clear outputs
MF35	BMB 6-11 outputs

Terminals C, F, J, L, N, R, and U of these receptacles are grounded within the computer, and terminals D, E, H, K, M, P, S, T, and V carry signals. These terminals mate with Type W011 Signal Cable Connectors at each end of 93-ohm coaxial ribbon cable.

Interface connections to the PDP-8 for all peripheral equipment can be made with series cable connections between devices. Only one set of cables connects to the computer; two sets of cables connect to each I/O device. One set receives the computer connection from the computer or from the previous I/O device, and one set passes the connection to the next I/O device. Where physical location of equipment does not make series bus connections feasible, or when cable length becomes excessive, place additional interface connectors near the computer (such as just below the operator console in a cabinet configuration system).

All logic signals which pass between the PDP-8 and the I/O equipment are standard DEC levels or standard DEC pulses. Mnemonic names of logic signals indicate the assertion condition of the signal. Standard levels are either ground potential (0.0 to −0.3v) designated by an open diamond (——◇), or −3v (−3.0 to −4.0v) designated by a solid diamond (——◆). Standard pulses in the positive direction are designated by an open triangle (——▷), and negative pulses are designated by a solid triangle (——▶). Pulses originating in R and S series modules are positive-going pulses which start at −3v, go to ground for 100 nsec, then return to −3v. Pulses originating in W series modules are always negative, are always referenced to ground, are 2.5v in amplitude (2.3 to 3.0v) with a 2v overshoot, and are of 400-nsec duration. Computer input signals that drive the interface bus to ground (inputs to the AC, CLEAR AC, SKIP, INCREMENT MB, BREAK REQUEST, and INTERRUPT REQUEST) must be connected to the collector of a grounded-emitter transistor, and so can be considered to be transistor-gated negative pulses () or levels ().

LOADING AND DRIVING CONSIDERATIONS

All interface circuits within the PDP-8 consist of series R, S, or W FLIP CHIP modules. When interconnecting these circuits with those in the peripheral equipment, it is important to keep the load on each circuit within its driving ability.

Since a flip-flop consists of two cross-connected diode gates, all input circuits of series R and S modules consist of either a diode gate or a diode-capacitor-diode gate circuit. All inputs draw current from the same direction. Each diode gate input draws 1 ma, and the diode gate output drives a 20-ma load. The internal load resistor draws 2 ma in series R modules, and 5 ma in series S modules. Therefore, a diode gate in an R series module with a clamped load resistor can drive an 18-ma load. The direct set and clear terminals of flip-flops draw 1 ma. The output capability of a series R flip-flop is 20 ma less 2 ma for the load resistor permanently connected in the flip-flop, and 1 ma for conditioning the opposite side of the flip-flop. The flip-flop can drive a 17-ma external load.

The DCD gates on flip-flops and pulse amplifiers draw 2 ma at level inputs and 3 ma at pulse inputs. When two DCD gates drive both sides of the same flip-flop, the load on both pulse inputs totals only 4 ma. When the level inputs are connected together as in a complement configuration, the total input load is only 3 ma.

Capacitive loading adversely affects the performance of series R and S modules; therefore, where long lines are being driven, extra clamped loads should be added to sufficiently discharge the cable capacitance. As a general rule, an extra 2 ma of clamped load current should be added for every foot of wire beyond 1-1/2 feet. An exception to this rule is the R650 Bus Driver module. This module can drive

coaxial cable of 100-ohm characteristic impedance through a series driving resistor. If coaxial cable is not used, use the direct output provided that the lines are short. If reflections occur on the line, adjust the resistive output of the bus driver to correct the problem. Shunt termination on the far end of the transmission line is not advisable.

The Type R650 Bus Driver module has two types of outputs: the fast and the slow (or ramp) output. Using the fast output, the bus driver operates merely as a fast amplifier. When the ramp output is used, an integrating capacitor inserted between the input of the bus driver and the output stage causes the output lines to move from ground to −3v, or in the reverse direction, in approximately 500 nsec. This connection, used on the AC lines, helps to reduce cross-talk. All other Type R650 Bus Driver module outputs are fast.

Terminate the Type W640 Pulse Amplifier modules carefully. If the output of these modules generates sufficient noise, regeneration may result. For this reason, output lines of Type W640 Pulse Amplifier modules should be well shielded. The outputs of these modules are either 400 nsec or 1 μsec in width. All connections on the standard PDP-8 use the 400-nsec pulse width.

Input circuits to the PDP-8 consist, in many cases, of a 10-ma clamped load and a direct input to a flip-flop or pulse amplifier. The input load is 10 ma for the clamped load and 1 ma for the flip-flop or the pulse amplifier. Give careful consideration to capacitive loads on the input lines, since the input lines must be at −3v before the pulse amplifier or flip-flop begins its next machine cycle.

The machine itself usually determines timing. However, the following timing considerations apply to the modules. The Type S111 Diode Gate sets up in approximately 50 nsec in either direction under normal load conditions. Fall times are faster with heavier loads, and the best method to speed up a slow diode gate is to connect an external load across the input to ground. The DCD gates set up in 400 nsec, as measured from the end of the preceding 100-nsec pulse, and both the level and pulse inputs must return to −3v for 400 nsec before the next pulse is applied. Series R and S pulses are 100 nsec in width, measured from the 10-percent point of the leading edge to the 90-percent point of the trailing edge. Fall time is not critical on these pulses, provided that the pulse has returned to −3v in time to come up for the next pulse.

PROGRAMMED TRANSFER INTERFACE

Tables 6-1 and 6-2 summarize input and output interface signal connections for use in programmed operations.

TABLE 6-1 PROGRAMMED TRANSFER INPUT INTERFACE

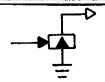
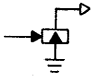
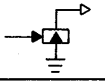
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
AC 0		PE2D	PA7, PB7 AE	R210	AC	BS-D-8P-0-2
AC 1		PE2E	PA8, PB8 AE	R210	AC	BS-D-8P-0-2
AC 2		PE2H	PA9, PB9 AE	R210	AC	BS-D-8P-0-2
AC 3		PE2K	PA10, PB10 AE	R210	AC	BS-D-8P-0-2
AC 4		PE2M	PA11, PB11 AE	R210	AC	BS-D-8P-0-2
AC 5		PE2P	PA12, PB12 AE	R210	AC	BS-D-8P-0-2
AC 6		PE2S	PA13, PB13 AE	R210	AC	BS-D-8P-0-2
AC 7		PE2T	PA14, PB14 AE	R210	AC	BS-D-8P-0-2
AC 8		PE2V	PA15, PB15 AE	R210	AC	BS-D-8P-0-2
AC 9		PF2D	PA16, PB16 AE	R210	AC	BS-D-8P-0-2
AC 10		PF2E	PA17, PB17 AE	R210	AC	BS-D-8P-0-2
AC 11		PF2H	PA18, PB18 AE	R210	AC	BS-D-8P-0-2
CLEAR AC		PF2P	PA19J	S603	AC Control	BS-D-8P-0-3

TABLE 6-1 PROGRAMMED TRANSFER INPUT INTERFACE (continued)

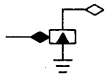
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
INTERRUPT REQUEST		PF2M	PD36K	S111	Program Interrupt Sync.	BS-D-8P-0-10
SKIP		PF2K	PB21V	S603	Skip Control	BS-D-8P-0-10

TABLE 6-2 PROGRAMMED TRANSFER OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BAC 0 (1)		ME34D	ME26J	R650	I/O Buffers	BS-D-8M-0-16
BAC 1 (1)		ME34E	ME26T	R650	I/O Buffers	BS-D-8M-0-16
BAC 2 (1)		ME34H	ME27J	R650	I/O Buffers	BS-D-8M-0-16
BAC 3 (1)		ME34K	ME27T	R650	I/O Buffers	BS-D-8M-0-16
BAC 4 (1)		ME34M	ME28J	R650	I/O Buffers	BS-D-8M-0-16
BAC 5 (1)		ME34P	ME28T	R650	I/O Buffers	BS-D-8M-0-16
BAC 6 (1)		ME34S	MF26J	R650	I/O Buffers	BS-D-8M-0-16
BAC 7 (1)		ME34T	MF26T	R650	I/O Buffers	BS-D-8M-0-16
BAC 8 (1)		ME34V	MF27J	R650	I/O Buffers	BS-D-8M-0-16
BAC 9 (1)		MF34D	MF27T	R650	I/O Buffers	BS-D-8M-0-16
BAC 10 (1)		MF34E	MF28J	R650	I/O Buffers	BS-D-8M-0-16

TABLE 6-2 PROGRAMMED TRANSFER OUTPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BAC 11 (1)	—◇	MF34H	MF28T	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (0)	—◇	ME35K	MC27T	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (1)	—◇	ME35M	MC28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (0)	—◇	ME35P	MC28T	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (1)	—◇	ME35S	MC29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (0)	—◇	ME35T	MC29T	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (1)	—◇	ME35V	MD25J	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (0)	—◇	MF35D	MD25T	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (1)	—◇	MF35E	MD26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (0)	—◇	MF35H	MD26T	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (1)	—◇	MF35K	MD27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (0)	—◇	MF35M	MD27T	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (1)	—◇	MF35P	MD28J	R650	I/O Buffers	BS-D-8M-0-16
IOP 1	—▶	MF34K	MC31H	W640	I/O Buffers	BS-D-8M-0-16
IOP 2	—▶	MF34M	MC31N	W640	I/O Buffers	BS-D-8M-0-16
IOP 4	—▶	MF34P	MC31U	W640	I/O Buffers	BS-D-8M-0-16

Accumulator Data Input (2)

The AC input receives data transferred from an I/O device to the PDP-8. For a data transfer from an I/O device, the CLEAR AC signal first clears the AC flip-flops; then the input signals from the I/O device arrive directly at the set input of the AC flip-flops. A positive pulse that drives any input line to ground sets a binary 1 into the associated AC flip-flop. Each AC input presents a 10-ma clamped load and a 1-ma direct input to the flip-flop.

Clear AC Input (3)

An interface connection to the PDP-8 allows a programmed I/O device to clear the AC. In this way an external device supplying information to the computer ensures that the word being read into the AC is not transferred in over an existing word. Transferring a word into the AC without first clearing the AC results in the inclusive OR of the new word, with the previous word being held in the AC after the transfer. The CLEAR AC signal initiates operation of the Type S603 Pulse Amplifier module at location PA19 by driving the input terminal to ground. The pulse amplifier may be triggered by a standard DEC positive pulse of 100-nsec duration or by a positive-going transition with a rise time of less than 60 nsec supplied to this input. This connection presents a clamped 10-ma load and a 1-ma diode load to the pulse source.

Program Interrupt Request Input (10)

Signals from I/O devices which interrupt the program in progress are connected to a bus in the PDP-8. Connections to this bus must be static levels: ground level to interrupt; −3v for no effect. The INTERRUPT REQUEST signal is clamped at −3v by a 10-ma clamped load in the W005 Clamped Load module at location PE9. The S111 Diode Gate module at location PD36 inverts and isolates the signal which then arrives as one input to the S111 Diode Gate module at location PC35 to initiate the internal interrupt gate. The INTERRUPT REQUEST signal source must be capable of driving a 10-ma clamped load plus the 1-ma input load of the diode gate module.

Input/Output Skip Input Connection (10)

A skip bus is available for input connections to the PDP-8 from gated SKIP pulses generated in I/O equipment. A flag or device status level which is strobed or sampled by an IOT pulse usually produces input SKIP pulses. The IOT pulse from the device selector strobes the flag; and, if it is in the preselected binary condition, the instruction following the IOT is skipped.

The input SKIP pulses drive one input of the Type S603 Pulse Amplifier module at location PB21 to ground. The pulse source must be capable of driving a 10-ma clamped load and the 3-ma load represented by the pulse input of the pulse amplifier.

Buffered AC Data Output (16)

Data contained in the AC as static levels supplies information to I/O devices. These static levels can be strobed into an I/O device register by IOT pulses from the associated device selector. The static level of each buffered AC output signal is at −3v when the bit contains a binary 0 and at ground potential when that bit contains a binary 1.

The BAC signals arrive at the interface connections through Type R650 Bus Driver modules at locations ME26 through ME28 and MF26 through MF28. To avoid the possibility of ringing on long interface lines, the bus driver connections provide a total transition time of 800 nsec for output rise and 700 nsec for output fall. The bus drivers for bits 0 through 3 can drive a 20-ma load; the bus drivers for bits 4 through 11 also drive the teleprinter, thereby reducing the external driving capability to 18 ma.

Buffered MB Select Code Output (16)

Bits 3 through 8 of an IOT instruction held in the MB select the I/O device addressed by the instruction. Complementary output signals from flip-flops MB3-8 supply the input to each device selector in the external I/O device through Type R650 Bus Driver modules at locations MC25 through MC29 and MD25 through MD29. The binary 1 outputs also serve as data word outputs during a data break. Each BMB signal at ground potential can drive a 20-ma load.

IOP Generator Output (16)

The IOP 1, IOP 2, and IOP 4 pulses trigger pulse amplifiers in the addressed peripheral equipment device selector. When triggered, the pulse amplifiers produce IOT pulses which perform control functions in the peripheral equipment or in the processor. Type W640 Pulse Amplifier modules at location MC31 standardize the IOP pulses prior to application to the interface connections. Each pulse output can drive a 10-ma load.

DATA BREAK INTERFACE

Tables 6-3 and 6-4 summarize the input and output interface connections used in data break transfers.

TABLE 6-3 DATA BREAK INPUT INTERFACE

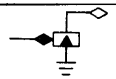
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
DATA ADDR 0 (1)	—◇	PE3D	PC7, PD7 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 1 (1)	—◇	PE3E	PC8, PD8 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 2 (1)	—◇	PE3H	PC9, PD9 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 3 (1)	—◇	PE3K	PC10, PD10 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 4 (1)	—◇	PE3M	PC11, PD11 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 5 (1)	—◇	PE3P	PC12, PD12 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 6 (1)	—◇	PE3S	PC13, PD13 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 7 (1)	—◇	PE3T	PC14, PD14 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 8 (1)	—◇	PE3V	PC15, PD15 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 9 (1)	—◇	PF3D	PC16, PD16 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 10 (1)	—◇	PF3E	PC17, PD17 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 11 (1)	—◇	PF3H	PC18, PD18 CR	R211	MA	BS-D-8P-0-4
DATA BIT 0 (1)	—◇	PE4D	PC7, PD7 DM	R211	MB	BS-D-8P-0-5

TABLE 6-3 DATA BREAK INPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
DATA BIT 1 (1)	—◇	PE4E	PC8, PD8 DM	R211	MB	BS-D-8P-0-5
DATA BIT 2 (1)	—◇	PE4H	PC9, PD9 DM	R211	MB	BS-D-8P-0-5
DATA BIT 3 (1)	—◇	PE4K	PC10, PD10 DM	R211	MB	BS-D-8P-0-5
DATA BIT 4 (1)	—◇	PE4M	PC11, PD11 DM	R211	MB	BS-D-8P-0-5
DATA BIT 5 (1)	—◇	PE4P	PC12, PD12 DM	R211	MB	BS-D-8P-0-5
DATA BIT 6 (1)	—◇	PE4S	PC13, PD13 DM	R211	MB	BS-D-8P-0-5
DATA BIT 7 (1)	—◇	PE4T	PC14, PD14 DM	R211	MB	BS-D-8P-0-5
DATA BIT 8 (1)	—◇	PE4V	PC15, PD15 DM	R211	MB	BS-D-8P-0-5
DATA BIT 9 (1)	—◇	PF4D	PC16, PD16 DM	R211	MB	BS-D-8P-0-5
DATA BIT 10 (1)	—◇	PF4E	PC17, PD17 DM	R211	MB	BS-D-8P-0-5
DATA BIT 11 (1)	—◇	PF4H	PC18, PD18 DM	R211	MB	BS-D-8P-0-5
BREAK REQUEST	⏚◇	PF3K	PC32J	S203	Major State Gen.	BS-D-8P-0-6
TRANSFER DIRECTION	—◆ *	PF3M	PD23E	S111	MB Control	BS-D-8P-0-5

*Direction is into PDP-8 when signal is −3v, out of PDP-8 when ground potential.

TABLE 6-3 DATA BREAK INPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
INCREMENT MB		PF3T	PD31M	S107	MB Control	BS-D-8P-0-5
CYCLE SELECT		PF4K	PE7S	S107	Major State Gen.	BS-D-8P-0-6
INCREMENT CA**		PF4M	PE10F	R121	MB Control	BS-D-9P-0-5

**This signal must not be −3v unless PDP-8 is in break state.

TABLE 6-4 DATA BREAK OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BMB 0 (1)		ME35D	MC26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 1 (1)		ME35E	MC26T	R650	I/O Buffers	BS-D-8M-0-16
BMB 2 (1)		ME35H	MC27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (1)		ME35M	MC28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (1)		ME35S	MC29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (1)		ME35V	MD25J	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (1)		MF35E	MD26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (1)		MF35K	MD27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (1)		MF35P	MD28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 9 (1)		MF35S	MD28T	R650	I/O Buffers	BS-D-8M-0-16

TABLE 6-4 DATA BREAK OUTPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BMB 10 (1)	—◇	MF35T	MD29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 11 (1)	—◇	MF35V	MD29T	R650	I/O Buffers	BS-D-8M-0-16
B BREAK	—◆	PF3P	PE8T	R650	Major State Gen.	BS-D-8P-0-10
ADDRESS ACCEPTED	—▷	PF3S	PF10H	W640	MA Control	BS-D-8P-0-10
WC OVERFLOW	—▶	PF4P	PF10N	W640	MB Control	BS-D-8P-0-10

Data Address Inputs (4)

Address signals arrive at the MA during a data break to designate the core memory address of the transfer. These DATA ADDR signals condition a pair of DCD gates at the input of each MA flip-flop and are at ground potential to signify a binary 1. A DATA ADDR signal travels directly to the gate at the 1 input and through an inverter to the gate at the 0 input, thereby providing a jam transfer. The DATA ADDR signals must arrive during T2 of the cycle preceding the data break cycle. To assure proper timing, these signals should occur concurrently with the BREAK REQUEST signal. Each DATA ADDR signal connection presents a 3-ma (maximum) load to the signal source in the I/O device.

Data Bit Inputs (5)

Input connections to the MB are also made through the interface connections. These connections are made to the DATA BIT level input of a DCD gate in each module of the MB. Data supplied to the MB inputs must be at ground level to specify a binary 1, or must be −3v for a binary 0. The DATA ⟶ MB pulse strobes this data into the MB flip-flops, as described in connection with the TRANSFER DIRECTION signal description. Each DATA BIT signal input represents a 2-ma load to the signal source.

Data Break Request Input Signal (6)

The break state is entered to transfer information between a peripheral device and the core memory via the MB. This state is entered only after the external device supplies a ground-level BREAK REQUEST signal to the computer. The signal is applied to one input of a DCD gate in the S203 Triple Flip-Flop module at location PC32. The second input to this gate is the T1 pulse that strobes the BREAK REQUEST signal into a synchronizing flip-flop. This flip-flop is sampled and cleared during T2 of each cycle. The BREAK REQUEST signal interface input must drive a 10-ma clamped load to the level input of a DCD gate, which represents a 2-ma load at ground.

Transfer Direction Input Signal (5)

A TRANSFER DIRECTION signal must arrive at the computer during time state T2 of the cycle preceding a break state, to determine the read or write status of the memory for the data break. At ground potential this signal specifies a transfer from the core memory to the I/O device; at −3v the signal specifies a transfer into core memory from the external device. This signal must be at ground potential before T2 of the preceding cycle or no MEMORY STROBE pulse occurs, and data cannot transfer out of core memory. If the signal is at −3v, the DATA ⟶ MB pulse occurs during T1 of the break state, and the data arriving at the MB inputs is strobed into the MB flip-flops. One input of a 2-input NAND gate in the Type S111 Diode Gate module at location PD23 receives the TRANSFER DIRECTION signal. The BREAK

signal supplies the second input to the gate so that the TRANSFER DIRECTION signal has effect only when the computer is in the break state. The input represents a 1-ma load to the TRANSFER DIRECTION signal source.

Increment MB Input Signal (5)

An INCREMENT MB signal input to the PDP-8 allows the contents of device-specified core memory location to increment by 1 during a data break. This input requires a ground level signal that is gated to occur only when the B BREAK signal is present. The Type S107 Inverter module at location PD31 receives this signal. Connection to this point presents a 1-ma load on the driving source of the INCREMENT MB signal.

Cycle Select Input Signal (6)

A device requesting a data break must supply a CYCLE SELECT signal to specify that a single-cycle or a 3-cycle break is needed. An S107 module that exhibits a load of 1 ma at ground and no load at −3v receives this signal. When this signal is at ground potential, a 3-cycle break is requested; when it is at −3v, a 1-cycle break is requested.

Increment CA Input Signal (5)

During the current address (CA) cycle of a 3-cycle data break the address of the transfer can be incremented by 1 so that data break transfers occur at successive core memory locations. The INCREMENT CA signal which arrives from the requesting device determines incrementation of the address during the CA state. If the signal is at −3v the address increments; if it is at ground the address does not increment. This signal must occur at the beginning of the CA state (T2 time), arriving at a gate of a Type R121 module whose ground-level output enables a DCD gate that is triggered by a T1 pulse. When triggered, this gate causes the COUNT MB pulse to advance the address contained in the MB. At ground potential the INCREMENT CA signal source receives 1 ma of load and at −3v it receives no load.

Buffered MB Data Output (16)

Type R650 Bus Driver modules isolate and power amplify the binary 1 output of each MB flip-flop. During a data break in which the transfer direction is out of the computer, words transfer from core memory to the I/O device via these bus drivers. These bus driver outputs for bits MB3-8 arrive at the device selectors for programmed data transfers. Each BMB output signal is at ground potential to signify a 1, and is capable of driving a 20-ma load.

Buffered Break State Output Signal (10)

When in the break state, the computer supplies a negative signal level to external devices. This −3v signal is often logically combined with a timing pulse to initiate operations in an I/O device. This signal level arrives at the interface connections through the Type R650 Bus Driver module at location PE8. The bus driver output is capable of driving a 20-ma load.

Address Accepted Output (10)

During time state T2 of each break state cycle, the PDP-8 produces a standard DEC 400-nsec positive pulse when the externally supplied address is strobed into the MA. The W640 Pulse Amplifier module at location PF10 produces this ADDRESS ACCEPTED pulse, which can drive a 10-ma load.

WC Overflow Output Pulse (10)

During the word count (WC) cycle of a 3-cycle data break, the word count reads into the MB from core memory, increments by 1, and is rewritten in memory. Incrementation of the word count causes MB0 to change from the 1 to the 0 state, generating the WC OVERFLOW pulse and transmitting it to the device using the data break. Usually the word count is preset to a negative number that is one less than the desired number of data break transfers. In this manner the WC OVERFLOW pulse indicates to the device that the current break will complete the desired number of transfers.

The WC OVERFLOW pulse is a standard DEC negative 400-μsec pulse produced by a Type W640 module. The pulse occurs approximately 80 μsec after memory strobe and can drive a 10-ma load.

MISCELLANEOUS INTERFACE

The PDP-8 interface has available several input and output signal connections which are not required for either programmed or data break transfers, but which peripheral equipment can use with either transfer mode. These connections are summarized in Tables 6-5 and 6-6.

Analog Input Signal

The Type 189 Analog-to-Digital Converter option receives an analog input signal between 0 and −10v. A BNC connector mounted on the outside of the processor fan housing at the back of the computer provides connection for this signal. Internal wiring cables this connector to the input of a Type A502 Comparator module. This module compares the analog input signal with a 0 to −10v analog signal which Type A601 and A604 Digital-Analog Converter modules produce. The input draws up to 1 μa depending on the relative polarity of the two voltage inputs of the A502 module. The maximum current difference between positive and negative input voltages is 1 μa. The difference input capacitance is 75 pf.

TABLE 6-5 MISCELLANEOUS INPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
ANALOG IN	→	Special*	PE11N	A502	A-D Conv	BS-D-189-0-2
LINE (1)	◆→	PF2V	PE6K, PE5L	S107, R123	DLI	BS-D-681-0-2
ADDR EXT 1	◇→	ME30D	ME8K, MC3K	S107, S151	Mem Ext Cont	BS-D-183-0-3
ADDR EXT 2	◇→	ME30E	ME8H, MC3E	S107, S151	Mem Ext Cont	BS-D-183-0-3
ADDR EXT 3	◇→	ME30H	ME8E, MC3J	S107, S151	Mem Ext Cont	BS-D-183-0-3

*Input connection to Type 189 Analog-to-Digital Converter is made at BNC connector mounted on back of processor fan housing.

TABLE 6-6 MISCELLANEOUS OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
TT INST	◆→	PF2T	PE6N	S107	DLI	BS-D-681-0-2
B RUN (1)	◆→	PF2S	PE8J	R650	Run Control	BS-D-8P-0-10
DF 0 (1)	◇→	ME30K	ME7L	S107	Mem Ext Cont	BS-D-183-0-3
DF 1 (1)	◇→	ME30M	ME7N	S107	Mem Ext Cont	BS-D-183-0-3
DF 2 (1)	◇→	ME30P	ME7R	S107	Mem Ext Cont	BS-D-183-0-3
BT1	→	MF34S	MD30H	W640	I/O Buffers	BS-D-8M-0-16
BT2A	→	MF34T	MD30U	W640	I/O Buffers	BS-D-8M-0-16
B POWER CLEAR	→	MF34V	MD30N	W640	I/O Buffers	BS-D-8M-0-16

LINE (1) Input and TT INST Output Signals

Addition of the Type 681 Data Line Interface option to the computer requires use of the LINE (1) input signal from the Type 685 Serial Line Multiplexer and the TT INST output signal to the 685.

The LINE (1) signal arrives at an inverter of an S107 module and two gates of an R123 module. This connection applies a load of 3 ma when the signal is at ground potential, and applies no load when the signal is at −3v.

The TT INST signal level is at −3v when a 681 instruction is being executed. This signal, produced in an S107 module, can drive 13 ma of external load when at ground potential.

Address Extension Inputs and Data Field Outputs

When the Type 183 Memory Extension Control is within the computer system, devices using the data break facility must supply a 12-bit data address and a 3-bit address extension. Conversely, the programmed transfer of an address to a register in a device that uses the data break occurs as a 12-bit word from the accumulator and a 3-bit data field extension from the 183.

The ADDRESS EXTENSION 1-3 signals must be ground potential to designate a binary 1 and −3v to designate a binary 0. An inverter of a Type S107 module and a Type S151 Binary-to-Octal Decoder module receive each of these signals. Each signal at ground potential has a load of 2 ma and each signal at −3v receives no load.

The DF 0-2 signals are constantly available at the interface connectors. They are flip-flop output signals buffered by an inverter of a Type S107 module. Each signal can drive 15 ma at ground potential, specifying a binary 1.

Buffered Run Output Signal (10)

Interface circuits supply the binary 1 output of the RUN flip-flop to external equipment. This signal is at −3v when the computer performs instructions and at ground potential when the program halts. Magnetic tape and DECtape equipment use this signal to stop transport motion when the PDP-8 halts, thus preventing the tape from running off the end of the reel. A Type R650 Bus Driver module at location PE8, which can drive a 20-ma load, routes the B RUN signal to the interface connector.

Buffered Timing Pulses BT1 and BT2A (16)

PDP-8 sends two buffered timing pulse signals, designated BT1 and BT2A, which synchronize operations between I/O devices and the computer. The timing signal generator circuits of the PDP-8 generate T1 and T2A

pulse signals, from which the BT1 and BT2 pulse signals derive. The Type W640 Pulse Amplifier module at location MD30 standardizes the T1 and T2A pulses as negative 400-nsec pulses. The resulting BT1 and BT2A pulses go to the interface connections. Interface cable connections for each of the pulse outputs can drive a 10-ma load.

Buffered Power Clear Pulse Output (16)

The POWER CLEAR pulses generated and used within the PDP-8 are made available at the interface connections. External equipment uses these pulses to clear registers and control logic during the power turnon period. Use POWER CLEAR pulses in this manner only when the logic circuits cleared by the pulses are energized before or at the same time the PDP-8 POWER switch is turned on.

The POWER CLEAR pulses, as used within the PDP-8, are DEC standard 100-nsec negative pulses (−3v to ground). These pulses occur during the interval between turnon of the POWER switch and the time at which the PWR STATUS signal from the power supply changes from ground to a −3v level or when the START key is pressed. The R401 100-KC Clock module at location PD30 generates the POWER CLEAR pulses at a 100-kc rate. The W640 Pulse Amplifier module at location MD30 standardizes these as negative 400-nsec pulses prior to application to the interface connection. The B POWER CLEAR interface cable connections can drive a 10-ma load.

DEVICE SELECTOR

Each peripheral device can contain one or more device selectors. A device selector can consist of a Type 4605 Pulse Amplifier system module; a Type W103 Device Selector FLIP CHIP module; or can be constructed of several modules such as the S603 Pulse Amplifier, S111 Diode Gate, and R002 Diode Cluster FLIP CHIP modules. Regardless of the circuit components, a device selector consists of a 6-input negative diode NAND gate, which is enabled only when the instruction contains the select code of the specified device. The select code arrives at the device selector inputs as the BMB levels. The output of the NAND gate enables gating circuits at the input of each of three pulse amplifiers, which the IOP 1, IOP 2, and IOP 4 pulses trigger.

Interface connections must supply inputs to each device selector from both the 1 and 0 outputs of MB bits 3-8 and from the three IOP pulse generator outputs. The output terminals of the device selector are then connected directly to the logic circuits of the I/O device, or to the computer SKIP or clear AC input busses.

CHAPTER 7

INSTALLATION

This chapter contains installation instructions for standard PDP-8 systems. The user should take notice of only those instructions and statements which apply to his equipment.

SITE PREPARATION

Space Considerations

Floor space for a basic optional computer cabinet is 22-1/4 inches wide (with two end panels) and 27-1/16 inches deep, plus any additional space for a table (see Figures 7-1 and 7-2). Figure 7-3 can be used in planning the installation of all I/O equipment mounted in standard computer cabinets, bearing in mind that other cabinets may or may not be equipped with a table at the operator console, and that cabinets bolted together in a multicabinet configuration are 19-3/4 inches wide with 1-1/4 inch end panels mounted on the outer ends. Minimum service clearance on all standard DEC computer cabinets is 8-3/4 inches at the front and 14-7/8 inches at the back. A standard DEC computer cabinet contains space for one mounting panel (two rows) of FLIP CHIP modules or an indicator panel above the computer, and contains space for three module mounting panels below the operator console. In either configuration the organization of the processor and the memory logic mounting frames is indicated on engineering drawings UML-E-8P-0-19 and UML-E-8M-0-20. The memory frame and the processor frame have hinges which provide access to the wiring side of the module mounting panels. Both of these frames extend beyond the back of the power supply in the table model to allow entrance of interface cables for connection to peripheral equipment. Cables enter the cabinet model through a port in the bottom of standard cabinets. Wheels and leveling devices on the cabinets allow cable clearance so that subflooring is not required.

The standard Teletype Automatic Send Receive set requires a floor space approximately 22-1/4 inches wide by 18-1/2 inches deep. Signal cable length restricts the location of the Teletype to within 18 inches of the side of the computer.

Environmental Conditions

No special environmental conditions need be met for proper operation of the PDP-8. Ambient termperature at the installation site can vary between 32 and 130°F (between 0 and 55°C) with no adverse effect on computer operation. However, to extend the life expectancy of the system, maintain the ambient temperature of between 70 and 85°F (21 and 30°C) at the installation site.

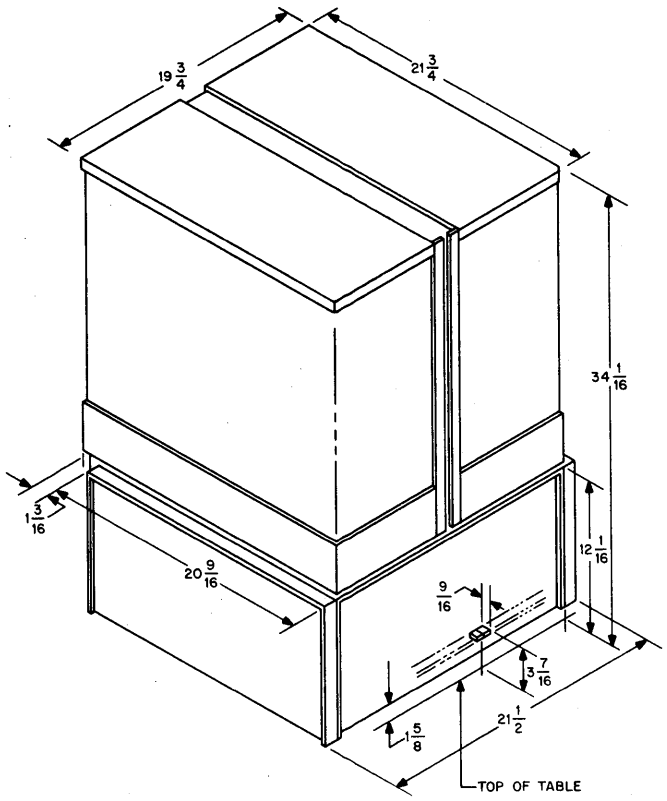


Figure 7-1 Table-Mounted PDP-8 Installation Dimensions

During shipping or storing of the system, the ambient temperature may vary between 32 and 130°F (0 and 55°C). Although DEC treats exposed surfaces of all cabinets and hardware against corrosion, avoid exposure of systems to extreme humidity for long periods of time.

Power Requirements

A standard PDP-8 operates from 115v (±17v), 60-cps (± 0.5 cps), single-phase power capable of supplying at least 15 amp. To allow connection to the power cable of the computer, this source should have a Hubbel 3-terminal, grounded-neutral flush receptacle (or its equivalent). A table-mounted PDP-8 comes with a 15-amp power plug; a rack-mounted PDP-8 has a 20-amp, twist-lock plug; and systems which draw more than 20 amps use a 30-amp, twist-lock plug. Power dissipation of a standard PDP-8 is approximately 780w, and the heat dissipation is approximately 2370 Btu/hr. Upon special request, a PDP-8 can be constructed to operate from a 220v (± 33v), 60-cps (± 0.5 cps), single-phase power source or from a 100v (±15v), 50-cps (± 0.5 cps), single-phase power source.

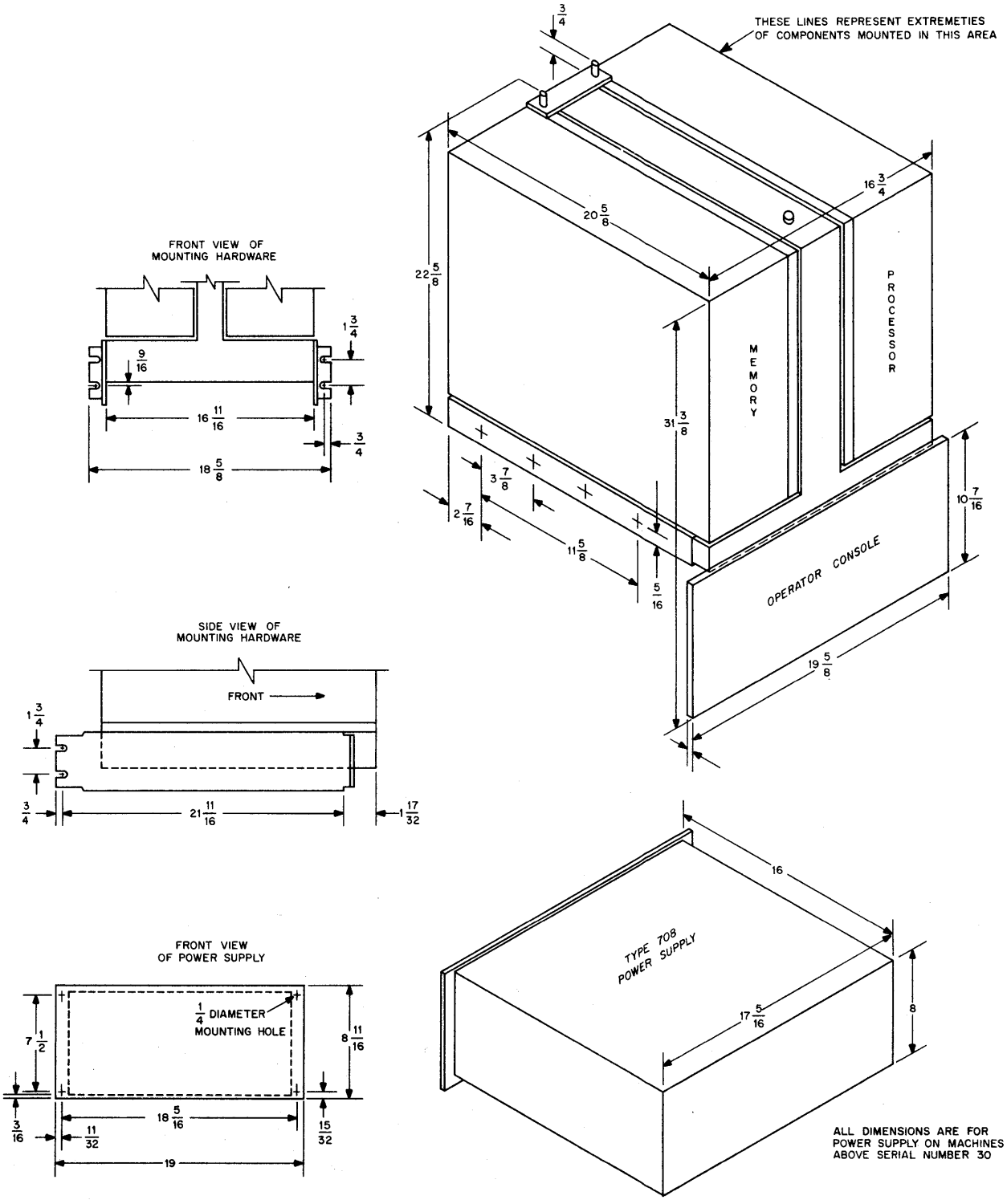


Figure 7-2 Cabinet-Mounted PDP-8 Installation Dimensions

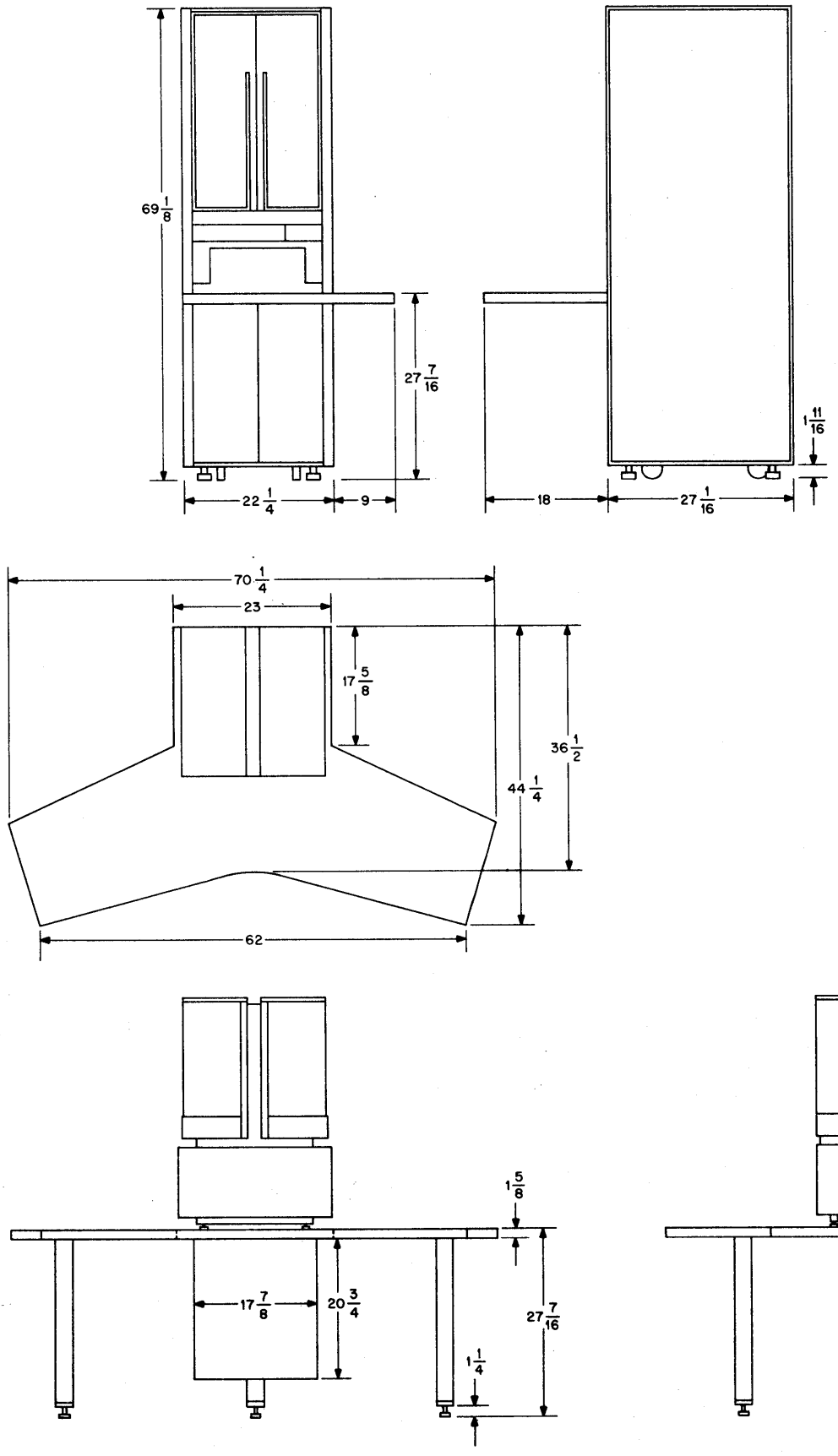


Figure 7-3 PDP-8 Optional Cabinet and Table Installation Dimensions

INSTALLATION PROCEDURE

Installation of a PDP-8 system requires no special tools or equipment. A fork-lift truck or other pallet-handling equipment and normal hand tools, including shears to cut the shipping straps, should be available for receiving and installing the equipment. To install the computer:

1. Place the computer package within the installation site near the final location. Cut the shipping straps and remove all packing material. Remove the table from the side of the cabinet, and remove the protector plate from the front of the cabinet. Open the rear doors, remove the shipping bolts which hold the plenum door closed, and open the plenum door. Remove the machine screw which holds each side of the cabinet to the pallet. Slide the cabinet off the pallet using a ramp (approximately 4-3/4 inches high) from the floor to the top of the pallet. Move the cabinet to its final location within the installation site.

2. Remove the tape which holds the modules in place within the mounting panels and the tape which holds the power cables to the floor of the cabinet. Assure that all modules are securely mounted in their connectors.

3. Remove the machine screw from the table mounting guide at each side of the back of the cabinet; install the table by passing the extension arms through the openings in the front of the cabinet and into the guides at the back of the cabinet; then replace the machine screws by passing them through the extension arms and turning them into the captive nut in each guide.

4. Open the Teletype carton and remove the packing material. Remove the back cover from the stand and remove and unwrap the copyholder, chad box, and power pack. Remove the stand from the shipping carton. Remove the Teletype console from the carton, holding it by means of the wooden pallet attached to the bottom. Remove the Teletype console from the pallet and mount it on the stand. Snap the power pack in place within the top front of the stand, and connect the Teletype console to the power pack (a six-lead cable attached at the console is connected to the power pack by means of a white plastic Molex 1375 Female Connector which mates with a male output plug on the power pack). Pass the three-wire power cable and the seven-conductor signal cable (which is terminated in a Type W070 FLIP CHIP™ Connector) through the opening at the lower left-hand corner of the Teletype stand; then replace the back cover of the stand by means of the two mounting screws.

5. Adjust the stabilizing feet on the four corners of the computer cabinet and on any I/O equipment. Adjust the leveling devices on the feet of the Teletype stand.

6. Remove the fan and filter assembly from the bottom of the DEC computer cabinet by disconnecting the captive screw at each side of the filter housing. Slide the rear portion of the cable port toward the rear door. Pass the larger diameter computer power cable out through the cable port; pass the Teletype signal and power cables into the cabinet through the cable port, and pass any other I/O equipment signal cables through the cable port; then replace the back half of the cable port and the fan and filter assembly.

7. Connect the three-prong male connector of the Teletype power cable to the recessed female connector at the rear of the computer power supply chassis.

8. Slide the PDP-8 memory-processor section forward in the DEC computer cabinet. Connect the Type W070 Connector of the Teletype signal cable to the mating connector of the PDP-8 at location MF30.

9. Set the PANEL LOCK switch to the full counterclockwise position. Set the POWER lock switch to the full counterclockwise position. Set the main power switch (circuit-breaker at rear of computer power supply chassis) to ON. Set the toggle switch (located to the right of the power input connector) to the up position.

10. Connect the female connector of the power supply cable to the recessed male connector at the rear of the power supply chassis. Connect the other end of this cable, the three-prong male connector, to the primary power source. The indicator on the rear panel should now be lit (indicating power is reaching the connector). Turn the POWER lock switch clockwise.

11. Install a roll of printer paper in the Teletype keyboard/printer, and install a tape in the punch as described in the Teletype technical manual or in Chapter 6 of this manual.

12. Set the LINE/OFF/LOCAL switch to LINE. Press the punch ON pushbutton. Strike several keys and note whether or not the printer and punch operate. Check the operation of the printer with the LINE/OFF/LOCAL switch set to LOCAL.

13. After completion of the checks, set the LINE/OFF/LOCAL switch to OFF.

14. Turn the POWER lock switch counterclockwise. Turn the PANEL LOCK switch clockwise.

This completes the installation of a standard PDP-8 system. Before commencing normal use, verify the operating capability of the system. Perform the power supply checks, and perform the marginal checks while running all of the diagnostic (Maindec) programs as described under Preventive Maintenance in Chapter 9 of this manual. Be sure to enter the margins obtained during each of these programs in the maintenance log since these levels are essential to determining rate of change in future preventive maintenance.

CHAPTER 8

OPERATION

CONTROLS AND INDICATORS

Keys and switches on the operator console provide manual control of the PDP-8 system. Visual indications of the machine status and the contents of the major registers and control flip-flops also appear on this console. Indicator lamps light to denote the presence of a binary 1 in specific register bits and control flip-flops. The functions of these controls and indicators are listed in Table 8-1, and their locations are shown in Figure 8-1. The functions of all controls and indicators of the Model 33-ASR Teletype unit as they apply to operation of the computer, are described in Table 8-2. The Teletype console is shown in Figure 8-2.

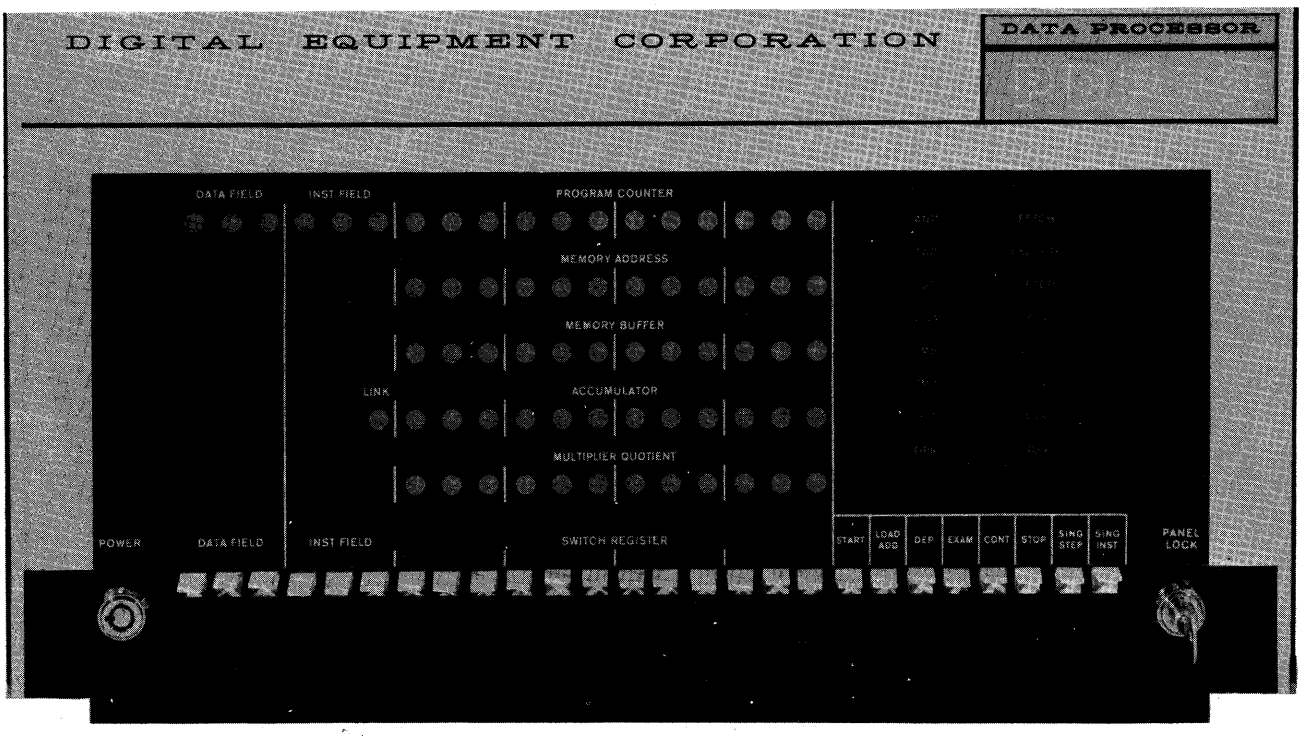


Figure 8-1 PDP-8 Operator Console

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS

Control or Indicator	Function
PANEL LOCK switch	When turned clockwise, this key-operated switch disables all keys and switches except the SWITCH REGISTER switches on the operator console. In this condition, inadvertent key operation cannot disturb the program. The program can, however, monitor the contents of the SR by execution of the OSR instruction.
POWER switch	This key-operated switch controls application of primary power to the computer. When turned clockwise, this switch applies primary power; when turned counterclockwise, it removes primary power.
START key	Starts the computer program by turning off the program interrupt circuits; clearing the AC, L, MB, and IR; setting the fetch state; transferring the contents of the PC into the MA; and setting the RUN flip-flop. Therefore, the word stored at the address currently held by the PC is the first instruction.
LOAD ADD key	Pressing this key sets the contents of the SR into the PC, sets the contents of the INST FIELD* switches into the IF, and sets the contents of the DATA FIELD* switches into the DF.
DEP key	Lifting this key sets the contents of the SR into the MB and core memory at the address specified by the current contents of the PC. This operation is performed by setting the execute state and forcing a DCA instruction. The contents of the PC are then incremented by one to allow storing of information in sequential core memory addresses by repeated operation of the DEP key.
EXAM key	Pressing this key sets the contents of the core memory at the address specified by the contents of the PC into the MB and AC. This operation is performed by clearing the AC, setting the execute state, and forcing a TAD instruction. The contents of the PC are then incremented by one to allow examination of the contents of the sequential core memory address by repeated operation of the EXAM key.
CONT key	Pressing this key sets the RUN flip-flop to continue the program in the state and instruction designated by the lighted console indicators, at the address currently specified by the PC.
STOP key	Causes the RUN flip-flop to be cleared at the end of the cycle in progress at the time the key is pressed.

*Activated only on systems containing the Type 183 Memory Extension Control option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
SING STEP key	Lifting this key causes the RUN flip-flop to be cleared to disable the timing circuits at the end of one cycle of operation. Thereafter, repeated operation of the CONT key steps the program one cycle at a time so that the operator can observe the contents of registers in each state.
SING INST key	Lifting this key clears the RUN flip-flop at the end of the next instruction execution. When the computer is started by pressing the START or CONT key, the SING INST key causes the RUN flip-flop to be cleared at the end of the last cycle of the current instruction. Thereafter, repeated operation of the CONT key steps the program one instruction at a time.
SWITCH REGISTER switches	Provide a means of manually setting a 12-bit word into the machine. Switches in the up position correspond to binary 1's; down, to 0's. Load the contents of this register into the PC by pressing the LOAD ADD key or load the contents into the MB and core memory by lifting the DEP key. Under program control, the OSR instruction can set the contents of the SR into the AC.
DATA FIELD indicators and switches*	The indicators denote the contents of the data field register (DF), and the switches serve as an extension of the SR to load the DF by means of the LOAD ADD key. The DF determines the core memory field of data storage and retrieval.
INST FIELD indicators and switches*	The indicators denote the contents of the instruction field register (IF), and the switches serve as an extension of the SR to load the IF by means of the LOAD ADD key. The IF determines the core memory field from which instructions are to be taken.
PROGRAM COUNTER indicators	Indicate the contents of the PC. When the machine is stopped, the contents of the PC indicate the core memory address of the first instruction to be executed when the operator presses the START or CONT key. When the machine is running, the contents of the PC indicate the core memory address of the next instruction.
MEMORY ADDRESS indicators	Indicate the contents of the MA. Usually, the contents of the MA denote the core memory address of the word currently or previously read or written. After operation of either the DEP or EXAM key, the contents of the MA indicate the core memory address just examined or deposited into.
MEMORY BUFFER indicators	Indicate the contents of the MB. Usually, the contents of the MB designate the word just read or written at the core memory address held in the MA.

*Activated only on systems containing the Type 183 Memory Extension Control option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
ACCUMULATOR indicators	Indicate the contents of the AC.
LINK indicator	Indicates the contents of the L.
MULTIPLIER QUOTIENT indicators**	Indicate the contents of the multiplier quotient (MQ). The MQ holds the multiplier at the beginning of a multiplication and holds the least-significant half of the product at the conclusion. It holds the least-significant half of the dividend at the start of division and holds the quotient at the conclusion.
Instruction indicators (AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR)	Indicate the decoded output of the IR as the instruction currently in progress.
FETCH, EXECUTE, DEFER, and BREAK indicators	Indicate the primary control state of the machine and the current memory cycle as a fetch, execute, defer, or break cycle, respec-pectively. (Word count and current address states are not indicated.)
ION indicator	Indicates the 1 status of the INT. ENABLE flip-flop. When lit, the interrupt control is enabled for information exchange with an I/O device.
PAUSE indicator	Indicates the 1 status of the PAUSE flip-flop when lit. The PAUSE flip-flop is set for 2.5 μsec by any IOT instruction that requires generation of IOP pulses and is reset at the end of this period. When the PAUSE flip-flop is set, it prevents the TG flip-flop from being complemented to prevent program advance beyond the current cycle.
RUN indicator	Indicates the 1 status of the RUN flip-flop. When lit, the internal timing circuits are enabled and the machine performs instructions.

**Activated only on systems containing the Type 182 Extended Arithmetic Element option.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS

Control or Indicator	Function
REL. pushbutton	Disengages the tape in the punch to allow tape removal or tape loading.
B. SP. pushbutton	Backspaces the tape in the punch by one space, allowing manual correction or rubout of the character just punched.
OFF and ON pushbuttons	Control use of the tape punch with operation of the Teletype keyboard/printer.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
START/STOP/FREE switch	Controls use of the tape reader with operation of the Teletype. In the lower FREE position, the reader is disengaged and can be loaded or unloaded. In the center STOP position, the reader mechanism is engaged but de-energized. In the upper START position, the reader is engaged and operated under program control.
Keyboard	Provides a means of printing on paper in use as a typewriter and punching tape when the operator presses the punch ON pushbutton. The keyboard also supplies input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position.
LINE/OFF/LOCAL switch	Controls application of primary power in the Teletype and controls data connection to the processor. In the LINE position, the Teletype is energized and connected as an I/O device of the computer. In the OFF position, the Teletype is de-energized. In the LOCAL position, the Teletype is energized for off-line operation, and signal connections to the processor are broken. Only line use of the Teletype requires that the computer be energized through the POWER switch if primary power for the Teletype is supplied from a source other than the outlet at the back of the computer.

OPERATING PROCEDURES

Many means are available for loading and unloading PDP-8 information. The means used depend upon the form of the information, time limitations, and the peripheral equipment connected to the computer. The following procedures are basic to any use of the PDP-8. Although these procedures are used infrequently as the programming and use of the computer become more sophisticated, they are valuable in preparing the initial programs and learning the function of machine input and output transfers.

Manual Data Storage and Modification

Programs and data can be stored or modified manually by means of the facilities on the operator console. The chief use of the manual data storage facility is to load the Readin Mode Loader program into the computer core memory. The Readin Mode Loader (RIM) is a program used for automatically loading into the PDP-8 other programs which have been assembled on perforated tape in RIM format. This program and the RIM tape format are described in the PDP-8 Users Handbook and in Digital Program Library descriptions. The RIM program is also listed in Table 8-3 for rapid reference and can be used as an exercise in manual data storage. To store data manually in the PDP-8 core memory:

Figure 8-2 Teletype Model 33-ASR Console

1. Turn the PANEL LOCK switch counterclockwise, and turn the POWER switch clockwise.

2. Set the bit switches of the SWITCH REGISTER (SR) to correspond with the address bits of the first word to be stored. Press the LOAD ADD key and observe that the address specified by the SR is held in the PC, as designated by lighted PROGRAM COUNTER indicators corresponding to switches in the 1 (up) position and unlighted indicators corresponding to switches in the 0 (down) position.

3. Set the SR to correspond with the data or instruction word to be stored at the address just set into the PC. Lift the DEP key and observe that the MB, and hence the core memory, hold the word set by the SR.

4. Observe that the contents of the PC have been incremented by 1 so that additional data can be stored at sequential addresses by repeated SR setting and DEP key operation.

To check the contents of an address in core memory, set the address into the PC as in step 2; then press the EXAM key. The MEMORY BUFFER and ACCUMULATOR lights indicate the address. The contents of the PC are incremented by 1 with the operation of the EXAM key, so that the operator can examine the contents of consecutive addresses by repeated operation after the original (or starting) address is loaded. He can modify any address by repeating both steps 2 and 3.

TABLE 8-3 READIN MODE LOADER PROGRAM

Address	Octal Content	Tag	Mnemonic	Comments
7756,	6032	BEG,	KCC	/CLEAR AC AND FLAG
7757,	6031		KSF	/SKIP IF FLAG = 1
7760,	5357		JMP .-1	/LOOKING FOR CHARACTER
7761,	6036		KRB	/READ BUFFER
7762,	7106		CLL RTL	
7763,	7006		RTL	/CHANNEL 8 IN AC0
7764,	7510		SPA	/CHECKING FOR LEADER
7765,	5357		JMP BEG+1	/FOUND LEADER
7766,	7006		RTL	/OK, CHANNEL 7 IN LINK
7767,	6031		KSF	
7770,	5367		JMP .-1	
7771,	6034		KRS	/READ, DO NOT CLEAR
7772,	7420		SNL	/CHECKING FOR ADDRESS
7773,	3776		DCA I TEMP	/STORE CONTENTS
7774,	3376		DCA TEMP	/STORE ADDRESS
7775,	5356		JMP BEG	/NEXT WORD
7776,	0	TEMP,	0	/TEMP STORAGE

Loading Data Under Program Control

Information can be stored or modified in the computer automatically only by enacting programs previously stored in core memory. For example, having the RIM Loader stored in core memory allows RIM format tapes to be loaded as follows:

1. Turn the PANEL LOCK switch counterclockwise, and turn the POWER switch clockwise.

2. Set the Teletype LINE/OFF/LOCAL switch to the LINE POSITION.

3. Load the tape in the Teletype reader by setting the START/STOP/FREE switch to the FREE position, releasing the cover guard by means of the latch at the right, loading the tape so that the sprocket wheel teeth engage the feed holes in the tape, closing the cover guard, and setting the switch to the STOP position. Load the tape in the back of the reader so that it moves toward the front as it is read. Proper positioning of the tape in the reader finds three channels being sensed to the left of the sprocket wheel and five channels being sensed to the right of the sprocket wheel.

4. Load the starting address of the RIM Loader program (7756_8) into the PC using the SR and the LOAD ADD key.

5. Press the computer START key and set the 3-position Teletype reader switch to the START position. The tape is read automatically.

The RIM Loader program automatically stores the Binary Loader (BIN) program as previously described. With the BIN Loader stored in core memory, program tapes assembled in Program Assembly Language (PAL III) binary format can be stored as described in the previous procedure, except that the starting address of the BIN Loader (7777_8) is used in step 4. After storing a program in this manner, the computer stops; the AC should contain all 0's if the program is stored properly. If the computer stops with a number other than 0 in the AC, a checksum error has been detected; therefore, the program has been stored incorrectly, and the storage procedure should be repeated. When the program has been stored correctly, initiate it by loading the program starting address (usually designated on the leader of the tape) into the PC using the SR and LOAD ADD key. Then press the START key.

Off-Line Teletype Operation

The Teletype can operate separately from the PDP-8 for typing, punching tape, or duplicating tapes. To use the Teletype in this manner:

1. Assure that the computer PANEL LOCK switch is turned counterclockwise, and turn the POWER switch clockwise if primary Teletype power is received from the outlet at the back of the computer. (For long periods of off-line Teletype use, connect the Teletype power cord to a separate source of 115v, 60-cps power.)

2. Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.

3. Load the punch as follows. Raise the cover and manually feed the tape from the top of the roll into the guide at the back of the punch. Advance the tape through the punch by manually turning the friction wheel; then close the cover.

4. Energize the punch by pressing the ON pushbutton, and produce about 2 ft of leader. The leader-trailer can be either 200_8 or 377_8 code. To produce the 200_8 code leader, simultaneously press and hold the CTRL and SHIFT keys with the left hand; press and hold the REPT key; press and release the key. When the required amount of leader has been punched, release all keys. To produce the 377_8 code leader, simultaneously press and hold both the REPT and RUB OUT keys until a sufficient amount of leader has been punched.

If an incorrect key is struck while punching a tape, the tape can be corrected as follows: If the error is noticed after typing and punching N characters, press the punch B. SP. (backspace) pushbutton N + 1 times and strike the keyboard RUB OUT key N + 1 times. Then continue typing and punching with the character which was in error.

To duplicate and obtain a listing of an existing tape: perform the procedure under the current heading. Then load the tape to be duplicated as described in step 2 of the procedure under Loading Data Under Program Control. Initiate tape duplication by setting the reader START/STOP/FREE switch in the START position. The punch and teleprinter stop when the tape being duplicated is completely read.

Corrections to insert or delete information on a perforated tape can be made by duplicating the correct portion of the tape and manually punching additional information or inhibiting punching of information to be deleted. This is accomplished by duplicating the tape and carefully observing the information being typed as the tape is read. In this manner, set the reader START/STOP/FREE switch to the STOP position just before the point of correction is typed. Punch information to be inserted on the keyboard. Delete information by pressing the punch OFF pushbutton and operating the reader until the portion of the tape to be deleted has been typed. It may be necessary to backspace and rub out one or two characters on the new tape if the reader is not stopped precisely on time. The number of characters to be rubbed out can be determined exactly by the typed copy. Be sure to count spaces when counting typed characters. Continue duplicating the tape in the normal manner after making the corrections.

New, duplicated, or corrected perforated tapes should be verified by reading them off line and carefully proofreading the typed copy.

Assembling Programs With PAL

Programs written in PAL symbolic language can be assembled into binary, machine-language program tapes by PAL as described in appropriate Digital Program Library documents. Basically, this operation is accomplished as follows:

1. Assure that the computer PANEL LOCK switch is turned counterclockwise, and turn the POWER switch clockwise.

2. Energize the Teletype by setting the LINE/OFF/LOCAL switch to the LINE position. Check the paper supply in the printer and punch and replenish as necessary.

3. Store the RIM Loader program as described under Manual Data Storage and Modification.

4. Store the BIN Loader program as described under Loading Data User Program Control.

5. Load the PAL program tape in the Teletype reader and set the START/STOP/FREE switch to the STOP position.

6. Load the starting address of the BIN Loader program (7777_8) into the PC using the SR and the LOAD ADD key.

7. Press the START key, set the Teletype reader switch to the START position, and wait until the tape has been completely read. When the tape stops, the AC should contain all 0's. If any ACCUMULATOR indicator is lit, a checksum error has been encountered, and this procedure should be repeated from step 5. Repeated errors indicate defects in the tape being read or in the operation of the PDP-8 system.

8. Load the symbolic tape into the reader and set the START/STOP/FREE switch to the STOP position.

9. Load the starting address of the assembler (200_8) into the PC using the SR and the LOAD ADD key.

10. Set bit 0 of the SR to the 0 position, and set bit 1 to the 1 position. These switch settings indicate to the program that the first pass of this two-pass assembler is to be performed.

11. Assure that the Teletype punch is turned off by pressing the OFF pushbutton.

12. Press the computer START key, start the tape reader by setting the three-position switch to the START position, and wait for the tape to be completely read and a symbol table to be typed. If an error printout is obtained at this time, correct the symbolic tape and repeat this procedure from step 8. If no error printout is obtained, proceed to step 13.

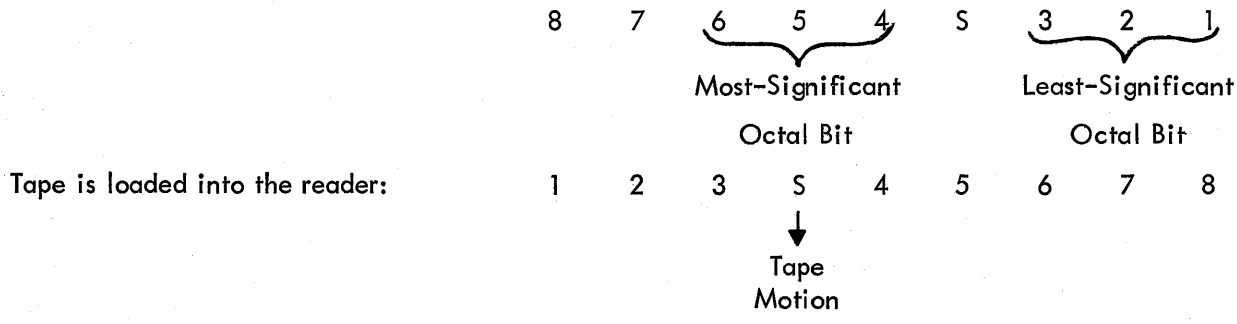
13. Remove and reload the tape in the reader.

14. Repeat step 9, then set SR bit 0 to 1 and bit 1 to 0 to indicate that the second pass is to be performed.

15. Press the Teletype punch ON pushbutton, press the START key, and wait until a leader is automatically punched. When leader punching stops, start the tape reader, and wait until the program stops. The perforated tape obtained in the second pass (reading) of the symbolic tape is an assembled binary tape which can be stored by means of the BIN Loader and can be run as described under Loading Data Under Program Control.

Teletype Code

The 8-bit code used by the Model 33-ASR Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. To convert the ASCII code to Teletype code, add 200 octal (ASCII + 200_8 = Teletype). This code reads in reverse of the normal octal form used in the PDP-8 since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore perforated tape is read:



The Model 33-ASR set can generate all assigned codes except 340 through 374 and 376. Generally, codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The Model 33-ASR set can detect all characters, but does not interpret all of the codes that it can generate as commands.

The standard number of characters printed per line is 72. The sequence for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations required to produce octal codes from 200 through 337, 375, and 377 are indicated in Table 8-4 with the associated ASCII character.

TABLE 8-4 TELETYPE CODE

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
220	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control ON	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control OFF	DC3	---	CTRL S
224	Device Control (~~TAPE~~)	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
233	Separator, Groups	S3	---	SHIFT CTRL K
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentation)	↑	↑	SHIFT
337	Left Arrow	←	←	SHIFT
340 through 374 are not available				
375	Unassigned Control	ⓘ	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

PROGRAMMING

Refer to the PDP-8 Users Handbook, F-85, for information on basic programming of the system. Refer to individual Digital Program Library documents (listed in Appendix 2) for specific information on the format, specifications, and procedures for using a particular program tape, such as Maindec or PAL.

CHAPTER 9

MAINTENANCE

Maintenance procedures for the PDP-8 consist of periodic preventive maintenance and malfunction corrective maintenance. Maintenance requires the equipment and test tapes listed in Table 9-1, or equivalent, as well as standard hand tools, cleansers, and test cables and probes.

TABLE 9-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547
Plug-in unit	Tektronix	Type 1A1
Clip-on current probe	Tektronix	Type P6016
X 10 Probe	Tektronix	P6008
Recessed tip, 0.065" for wire-wrap terminals	Tektronix	206-052
Current probe amplifier	Tektronix	Type 131
Hand unwrapping tool	Gardner-Denver	500130
Hand-operated wire-wrap tool with a 26263 bit for AWG wire and 18840 Sleeve	Gardner-Denver	14H1C
Potentiometric voltmeter*	John Fluke	Model 801H
Audio oscillator*	Hewlett Packard	Model 200CD
Plug-in unit*	Tektronix	Type L
FLIP CHIP Module Extender**	DEC	Type W980
Maindec 801 Instruction Test**	DEC	DEC-8-12-M
Maindec 802 Memory Checkerboard Test**	DEC	DEC-8-15-M

*Required only for the Type 189 Analog-to-Digital Converter option
**One is supplied with the equipment

TABLE 9-1 MAINTENANCE EQUIPMENT (continued)

Equipment	Manufacturer	Designation
Maindec 803 Address Test**	DEC	DEC-8-16-M
Maindec 810 Read Paper Tape Test**	DEC	DEC-8-13-M
Maindec 812 Punch Paper Tape Test**	DEC	DEC-8-14-M
Maindec 814 Teleprinter Test**	DEC	DEC-8-19-M
Paint spray can**	DEC	DEC Blue 5150-865
Paint spray can**	DEC	DEC Charcoal Brown
Air filter**	DEC	FIL-8
Filter-Kote**	Research Products Corporation	By name

**One is supplied with the equipment

Diagnostic programs, called Maindecs, exercise or test specific functions within the computer system. Maindec routines are paper tape programs in readin mode format. A detailed description of the program, procedures for its use, and information on analyzing the results to locate specific circuit failures accompany each tape. Use of these routines is indicated at the appropriate points in this manual as they apply to preventive or corrective maintenance on the standard PDP-8 system.

To insert or extract modules, first, turn off all power. To gain access to adjustment controls on the module or to points used in signal tracing, remove the module (use a straight, even pull to prevent twisting of the printed-wiring board) and insert a Type W380 FLIP CHIP Module Extender into the vacated module connector in the mounting panel. Then reinsert the module into the extender.

The procedures presented in this chapter assume that the reader understands the function of the keys and indicators on the operator console, and is familiar with machine programming as described in the PDP-8 Users Handbook, F-85.

In addition to the controls and indicators on the operator console and on the Teletype unit (described in Table 8-1 and Table 8-2), maintenance operations require the controls and indicators on the Type 708 Power Supply at the back of the computer (Figure 9-1) and on the lower frame inside each module mounting frame (see Figure 9-2). The function of these controls and indicators is described in Table 9-2.

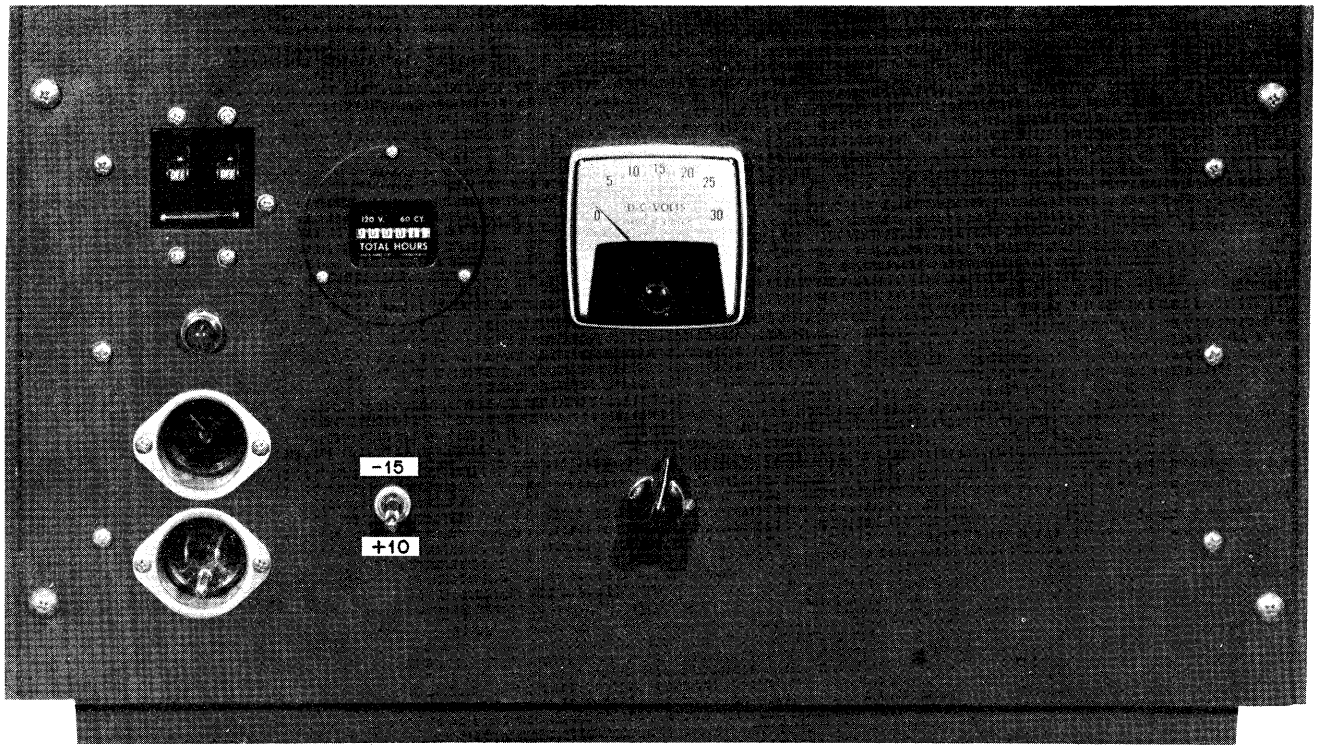


Figure 9-1 Power Supply Control Panel

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
	Power Supply
Circuit breaker	Protects the computer power source from overload due to failure of the computer power circuits.
Indicator lamp (red)	Lights to indicate the presence of primary power at the computer primary power input connector.
Female power connector	Primary power outlet for Teletype unit, maintenance, or auxiliary equipment.
Male power connector	Primary power input connection for computer.
Elapsed time meter	Indicates the cumulative total number of hours during which the computer has been energized and provides a unit of measure that is more appropriate than calendar time for determining preventive maintenance schedules.
−15/+10 switch	Controls the output of the marginal-check power supply. In the up position, the output is negative and is connected to the green −15 MC connector. In the down position, the output is positive and is connected to the orange +10 MC connector.

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
	Power Supply (continued)
Voltmeter	Indicates the output voltage of the marginal-check power supply in either polarity.
Control knob	Varies the amplitude of the marginal-check voltage between 0 and 20v.
	Module Mounting Door
MC/−15 switches	Select either the normal −15v power (from the blue connectors) or the negative output of the marginal-check supply (from the green connectors) for application to terminal B of all modules in the designated row.
MC/+10 switches and MC/SENSE AMP switch	Select either the normal +10v power (from the red connectors) or the positive output of the marginal-check supply (from the orange connectors) for application to terminal A of all modules in the designated row.
RESTART ON/OFF switch	When the KR01 option is included this switch on the processor frame enables or disables automatic restart of the program at restoration of computer primary power following a power failure.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed before initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks helps forestall incipient failures by discovering progressive deterioration and correcting minor damage at an early stage. Operators or maintenance personnel should record data obtained during preventive maintenance in a log book. Analysis of this data can indicate the rate of circuit deterioration and component degradation so that steps can be taken to prevent system failure.

Preventive maintenance tasks consist of mechanical checks, such as checking module seating, cleaning, and visual inspections; marginal checks, to aggravate any borderline circuit conditions or intermittent failures so that they can be detected and corrected; and checks of specific circuit elements such as the power supply, sense amplifiers and master slice control, and memory selectors. All preventive maintenance tasks should be performed as a function of existing conditions at the installation site. Perform the mechanical checks

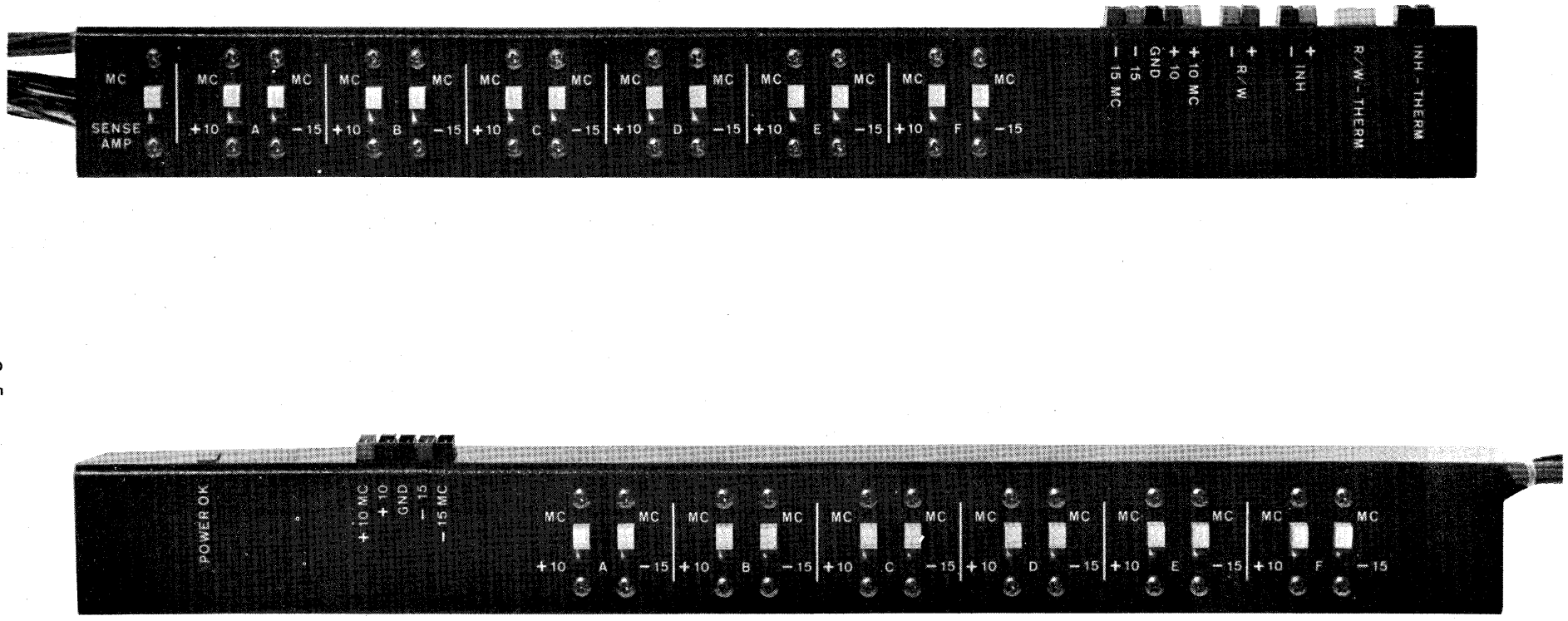


Figure 9-2 Marginal Check Switches (Memory Panel at Top and Processor Panel at Bottom)

at least once each month or as often as required, particularly cleaning to allow efficient functioning of the air filter. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. A typical recommended schedule is every 600 equipment operating hours or every four months, whichever occurs first.

The most important schedule to maintain is that of the simplest procedure--the mechanical checks. Many hours of computer downtime can be avoided by rigid adherence to a schedule based on the condition of the air filter. A dirty air filter can cause machine failure through overheating which has a number of deleterious effects.

Mechanical Checks

Ensure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filter. In a cabinet-model PDP-8, remove the filter at the bottom of the cabinet by removing the fan and housing, which are held in place by two knurled and slotted captive screws. In a table-model PDP-8, remove the metal strip just below the power supply control panel by removing the machine screw on both sides, then slide the filter out the back of the machine. (In the first 30 serial number computers in the table-top configuration, the filter lies on top of the power supply and is removed by unlocking and swinging open the module mounting panels.) Wash the filter in soapy water and dry it in an oven or by spraying it with compressed gas. Spray the filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin), and replace it in the computer.

3. Lubricate door hinges, slide mechanisms, and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC Blue Tweed Paint No. 5150-865 or DEC Charcoal Brown Paint.

5. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6. Inspect the following for mechanical security: keys, switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, capacitors, elapsed time meter, etc. Tighten or replace as required.

7. Inspect all module mounting panels to ensure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors that have these defects.

Power Supply Checks

Check the output voltage and ripple content of the 708 Power Supply as specified in Table 9-3. Use a multimeter to make these measurements without disconnecting the load. Use the oscilloscope to measure the p-p ripple content on all dc outputs of the supply. The +10 and −15 supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, the supply is considered defective and troubleshooting procedures are indicated. The inhibit and read/write supplies are adjustable but should be adjusted only in strict compilance with the memory current check procedures to obtain a specified memory drive current. These supplies are checked here only to provide a rough indication of output change since the last regularly scheduled preventive maintenance. Refer to engineering drawing RS-C-708.

TABLE 9-3 TYPE 708 POWER SUPPLY OUTPUTS

Measurement Terminals at Power Supply Output	Nominal Output DC Voltage	Output Voltage Range	Max. Output Current	Max. p-p Output Ripple
Blue TAB terminal	-15	-14.5 to -16.5 vdc	15 ma	700 mv
Red TAB terminal	+10	9.5 to +11.5 vdc	2 amp	700 mv
Orange (+) to green (-)	Marginal check	0 to 20 vdc	2 amp	700 mv
Orange (+) to green (-)	Inhibit supply (+35v)	27 to 37 vdc	2 amp	less than 50 mv*
Red (+) to blue (-)	Read/write supply (+35v)	27 to 37 vdc	1.5 amp	less than 50 mv*

*Supply is not within regulating range if ripple is more than 50 mv.

The inhibit and read/write supplies are regulated by their respective Type G808 Control modules and are temperature compensated by thermistors mounted at the load. This regulation is such that when the temperature of the load increases, the read/write and inhibit voltages decrease. Each Type G808 Control module may be adjusted by potentiometer R16, mounted on the control module. Clockwise rotation increases the read/write and inhibit currents.

When all supplies are operating normally, Control module G809 supplies a −3v power OK level. This module senses the −15v supply; if the supply potential drops below −14v or if the memory power supplies fail, the OK signal goes to ground potential, and contacts of relay K1 open to disconnect the read/write and inhibit supplies from the memory system.

Check the marginal-check voltages at the connectors located on the processor or memory marginal-check panel, or at the power supply marginal-check voltage output terminals.

1. Make sure all marginal-check switches are set to the normal voltage position.

2. Connect a multimeter between +10 MC terminal and GND.

3. Set the small toggle switch on the power supply control panel to the up position. Vary the marginal-check voltage by rotating the control located beneath the voltmeter on the control panel. Make full scale variations to ensure that a 20v range is attainable.

4. Observe that the voltmeter on the control panel and the multimeter correspond within ±1v at each discrete voltage setting.

5. Connect a multimeter between the −15 MC terminal and GND.

6. Set the toggle switch to the down position, and vary the marginal-check voltage as in step 3.

7. Observe corresponding voltages as in step 4.

8. Turn the voltage control fully counterclockwise; set the toggle switch to the center off position, and disconnect the multimeter.

Marginal Checks

Marginal checking uses Maindec diagnostic programs to test the functional capabilities of the computer while biasing the module operating voltages above and below the nominal levels within specified margins. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce

failures which are detected by the program. When the program detects an error, it usually provides a printout or visual indication to help locate the source of the fault and then halts. Therefore, marginal components can be replaced during scheduled preventive maintenance and forestall possible future equipment failure. If no marginal components exist, the operating voltages are biased beyond the specified margins, and the operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance, progressive deterioration can be observed and expected failure dates can be predicted. In this manner these checks provide a means of planned replacement. These checks are also useful as troubleshooting aids to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltages above +10v increases the transistor cutoff bias that must be overcome by the previous driving transistor; therefore low-gain transistors fail. Lowering the bias voltage below +10v reduces transistor base bias and noise rejection and thus provides a test to detect high-leakage transistors. Lowering this voltage also simulates high-temperature conditions (to check for thermal runaway). Raising and lowering the −15v supply increases and decreases the primary collector supply voltage for all modules and so affects output signal voltage.

Since marginal voltages attainable vary for different circuit changes and/or system configurations, determine the expected marginal-check voltages for a specific system from the initial factory test records and any subsequent test records in the maintenance log. A record of margins obtained at the factory for a specific system comes with each system and serves as a base for all preventive and corrective maintenance procedures. With time and nominal circuit operation deterioration, margins will decrease. This decrease does not affect reliable operation of the machine until there is little or no margin left. The normal slow rate of margin decay predicts the time at which the system should be refurbished to prevent sudden failure. Margins provide a measure of circuit performance and therefore can certify correct or defective operation. However, failure of a system to obtain the same margins year after year does not constitute a defect in the operation of the system. For example, if a specific margin decreases at the rate of 0.5v per year, no trouble is indicated. If this margin suddenly decreases by 0.7v in six months, troubleshoot to determine the cause of this rapid change.

CAUTION

Do not increase the −15v margin beyond −18v. Failure to observe this precaution may cause serious damage to the logic elements.

Marginal-check voltages arrive at both the processor and memory assemblies through connectors located on the bottom of each assembly. Use the control knob and voltmeter located on the control panel of the

708 Power Supply to adjust each marginal-check voltage from 0 to 20v. A toggle switch on this control panel selects either positive or negative marginal-check voltages. Power supply connectors are labeled on the marginal-check panels of the memory and processor assemblies. The color coding of the connectors at the side of each row of module options of a cabinet-model computer is as follows:

Connector	Voltage
Orange	+10v marginal check supply
Red	+10v normal fixed power supply
Black	ground
Blue	−15v normal fixed power supply
Green	−15v marginal check supply

SPDT switches on the marginal-check panel of the processor and the memory assembly distribute marginal-check and normal-supply voltages to each of six module rows in that assembly. The two positions for each SPDT switch are normal (down) and MC (up). Therefore, each module row may be marginally checked while all other rows maintain normal voltages.

To perform the checks:

1. Assure that all normal/marginal-check switches on each marginal-check panel are in the down position (+10, −15, or SENSE AMP).

2. Set the toggle switch on the marginal-check power supply to the +10 position (down).

3. Adjust the output of the marginal-check power supply so that the marginal-check voltmeter indicates 10v.

4. De-energize the computer; set the +10 normal/marginal switch for the first panel row to be checked to the MC/position (up); then restore power.

5. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the panel to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program from Table 9-4. To completely test the PDP-8, all Maindec programs listed in Table 9-4 should be performed at elevated and reduced voltages for each supply terminal (+10, −15) and for each module mounting panel indicated in the table.

TABLE 9-4 MARGINAL TEST PROGRAMS

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test							
	Instruction Test (801 Parts I and II)	Memory Checkerboard Test (802)	Address Test (803)	Read Paper Tape Test (810)	Punch Paper Tape Test (812)	Teleprinter Test (814)	Extended Arithmetic Element Test (801 Part III)	Memory Extension Control Test (801 Part IV)
PA	+10, −15							
PB	+10, −15							
PC	+10, −15							
PD	+10, −15							
PE							+10, −15	
PF							+10, −15	
SENSE AMP		+10						
MA*		+10, −15						
MB*		+10, −15						
MC		+10, −15	+10, −15					
MD		+10, −15	+10, −15					
ME				+10, −15	+10, −15	+10, −15		+10, −15
MF				+10, −15	+10, −15	+10, −15		+10, −15

*Note that when checking either the MA or the MB +10v line, the +10v normal/marginal switches for the SENSE AMP, MA, and MB must all be in the MC (up) position. When checking either the MA or MB −15v line, the −15v normal/marginal for both the MA and MB must be in the MC (up) position.

6. Decrease the marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal level (+10v).

7. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced. Readjust the marginal-check power supply to the nominal level (+10v).

8. De-energize the computer, and return the normal/marginal switch to the +10 position (down). Repeat steps 4 through 8 for the other panels to receive marginal checks of the +10v lines.

9. Repeat step 1 and energize the computer.

10. Set the toggle switch on the marginal-check power supply to the −15 position (up), and adjust the output until the marginal-check voltmeter indicates 15v.

11. De-energize the computer; set the −15 normal/marginal switch to the MC position (up) for the first panel row to be checked; restore power; then repeat step 5.

12. Repeat steps 6 and 7, readjusting the marginal-check power supply to the nominal −15v level at the end of each step. De-energize the computer; return the normal/marginal switches to the −15 position (down); then restore power.

13. Repeat steps 2 through 12 for each other module mounting panel row to be tested.

Memory Current Check

Measure and compare the memory currents with the values listed on the memory array label. This label indicates the optimum memory settings determined at the factory. Allow the equipment to warm up for approximately 1 hr before making measurements. Whenever possible, this check should be performed at an ambient temperature of 25°C. Compensate measured read/write and inhibit currents by subtracting 1 ma for every degree of ambient temperature above 25°C. (Add 1 ma for each degree below 25°C.)

Measure the read/write current using the oscilloscope and clip-on current probe at the yellow wire leading from the current-determining resistor to the Type G209 Memory Selector Switch. Synchronize the

oscilloscope with the negative transition of the READ signal found at location MC16D. Adjust the read/write current to the value specified on the memory array label by rotation of R16 in the Type G808 Read/Write Power Supply Control module. Clockwise rotation of R16 increases the read/write current.

In a similar manner, measure the inhibit current by connecting the clip-on current probe to a wire leading from the inhibit current determining resistor. See drawing BS-D-8M-0-15 for the appropriate inhibit terminal. Synchronize the oscilloscope on the negative transition of the INHIBIT (1) signal at terminal U of any of the Type G208 modules. Adjust the inhibit current to the value indicated on the memory array label. Clockwise rotation of R16 on the Type G808 Inhibit Power Supply Control module increases the inhibit current.

All current amplitude measurements should be made just before the knee in the curve at the trailing edge of a pulse.

Sense Amplifier Check

The Type G007 DC Sense Amplifier modules are adjusted for optimum efficiency through marginal-checking techniques. Perform the marginal checks on the +10v line of the sense amplifiers, using the Memory Checkerboard Program (MAINDEC 802). Adjust the slice level (potentiometer R3) of the Type G008 Master Slice Control module at location MR31 until approximately equal positive and negative margins can be obtained on the +10v line. Clockwise rotation of potentiometer R3 decreases the slicing level supplied to all the sense amplifiers.

Sense amplifiers are located at MA25 through MA30 and MB25 through MB30. Location MA31 contains the sense amplifier for the parity bit, and location MB31 contains the master slice control.

Type 189 Analog-to-Digital Converter Maintenance

The checks and adjustments presented in this portion of the manual apply only to PDP-8 systems containing the Type 189 option. Maintenance of the Type 189 involves program-repeated operation of the converter performed during each scheduled preventive maintenance to check accuracy and function of the option, and adjustment checks and procedures used to verify and/or adjust the operation of specific functional components. The functions checked by module are the timing of the Type R302 Delay modules, the −10v output of the Type A704 Precision Power Supply module, the adjustment of the ladder network in the Type A604 Digital-to-Analog Converter (DAC) modules, and the common balance and zero set of the Type A502 Difference Amplifier. Perform the timing checks and ladder network adjustments only when necessary as indicated by the converter check or by normal troubleshooting procedures. Check the

−10v reference supply and the difference amplifier approximately every 3 weeks or every 100 equipment operating hours, whichever occurs first. Maintenance of the Type 189 option requires the following equipment:

1. A potentiometric voltmeter which has infinite input resistance at null and which has an accuracy of ±0.01%.

2. A single-frequency sine wave source, between 30 and 100 cps. The output should be floating and the amplitude should be variable from 2 to 20 mv. The power source may be 115v 60-cycle suitably stepped down in amplitude.

3. A dc source of 5 ±0.5v for biasing the output of the sine wave source. This source can be a voltage divider connected across output terminals PE16C (ground) and PE16E (−10v).

4. A dual-trace oscilloscope having a vertical-deflection sensitivity of 5 mv or less per cm.

There are many ways to check and adjust the components of an analog-to-digital converter. Use of the information and procedures presented here can vary greatly depending on test equipment available and the object of the test or adjustment. The Analog-Digital Conversion Handbook, E-5100, published by DEC, gives additional background information and procedures for testing and adjusting converters.

Converter Check

This test repeatedly operates the converter by means of a 4-step program. Using a known analog input, the operator then verifies the conversion result displayed in the accumulator.

To perform the check:

1. Physically disconnect the normal analog input from the input to the Type 189 Converter. This connection is usually made with a BNC connector that can be disconnected. If the connection is made directly to the module connector, it must be broken at terminal PE11N.

2. Supply a known constant dc voltage to the input connector or to terminal PE11N. Obtain this potential by connecting a voltage divider across output terminals C (ground) and E (−10v) of the Type A704 Precision Power Supply at locations PE16 and PF16.

3. Store the following 4-instruction sequence into the computer core memory by means of the SWITCH REGISTER, LOAD ADD key, and DEP key on the operator console.

Address		Instruction	Mnemonic
BEG,	6000	6004	ADC
	6001	2250	ISZ
	6002	5201	JMP-1
	6003	5200	JMP BEG.

4. Start the program by loading the initial address into the PC using the SWITCH REGISTER and LOAD ADD key; then press the START key.

5. Record and compare the binary number in the accumulator with the value of the voltage connected in step 2. The answer in the accumulator is in 2's complement unsigned representation and can be converted to a decimal voltage value by using Table 9-5.

6. Repeat steps 2, 4, and 5 for several values of input voltage between 0.0 and −10v. Record the analog input signal and the binary answer obtained in each measurement. From these results determine if the answers obtained are within the limits specified by the accuracy connection of the converter or if the converter requires adjustment. If no adjustment is necessary, halt the program by pressing the STOP key; then remove the test connections made to the analog input, and restore the normal connection from the signal measured during programmed operation of this system.

Clock and Delay Timing Check and Adjustment

Check the timing of the Type R401 Clock and Type R302 Delay modules at locations PE13 and PE10, respectively, to assure that sufficient time is allowed for the conversion of each bit. To perform the check:

1. Connect the oscilloscope signal input to terminal PE15F; connect the trigger input to PE10V, and adjust for synchronizing on an external negative pulse.

2. Perform steps 3 and 4 of the previous procedure.

3. Observe that the pulse displayed on the oscilloscope is negative for 0.5 μsec and occurs at the prf listed under "Conversion Time per Bit" and occurs every 1.8 μsec plus the duration listed under the column "Instruction Execution Time" in Table 5-3 for the adjusted bit accuracy of the converter. Make any necessary adjustment in the pulse

TABLE 9-5 ANALOG-DIGITAL NUMBER CONVERSION

Unsigned Two's Complement Octal Number	Analog Voltage (Negative)
0000	0.
0001	0.00244140625
0002	0.0048828125
0004	0.009765625
0010	0.01953125
0020	0.0390625
0040	0.078125
0100	0.15625
0200	0.3125
0400	0.625
1000	1.25
2000	2.5
4000	5.
6000	7.5
7000	8.75
7400	9.375
7600	9.6875
7700	9.84375
7740	9.921875
7760	9.9609375
7770	9.98046875
7774	9.990234375
7776	9.9951171875
7777	9.99755859375
10000	10.

width by turning potentiometer R20 in the Type R302 Delay module at location PE10, or adjust the conversion time by turning the potentiometer R11 in the R401 module (accessible at the handle of module PE13).

Precision Power Supply Check and Adjustment

The −10v output of the Type A704 Precision Power Supply module at location PE16 and PF16 supplies the reference voltage used by the level amplifiers and determines the accuracy of the analog voltage generated by the converter ladder network. Use the oscilloscope to make a rough check of this adjustment. An accurate check or adjustment must be made with a high impedance instrument which is accurate to within at least 0.01%, such as the John Fluke potentiometric voltmeter. Adjust the supply within 1 min due to drifting of the voltmeter. To adjust the supply:

1. Connect a precision dc voltage to the analog input signal connector (− to PE11N, + or ground to PE11C) and set it to supply −9.99634v.

2. Start the program as in step 3 of the converter check.

3. Turn the screwdriver adjustment near the handle of the Type A704 module so that the digital value of the number in the accumulator alternates between 7776_8 and 7777_8. (This adjustment controls the setting of the fine control potentiometer R7 shown on schematic diagram RS-B-A704-3. The coarse control potentiometer R9 and the current control potentiometer R2 are preset at the factory and must not be adjusted in the field).

If a precision dc voltage supply is not available, use the following alternate procedure.

1. Calibrate the potentiometric voltmeter.

2. Connect the potentiometric voltmeter between terminals PE16C (ground) and PE16E or V (−10v).

3. Turn the screwdriver adjustment, accessible at the handle of the Type A704 module, until the voltmeter indicates −10.001 vdc ±0.1 mv.

If the output of the supply is 0.0v, check the external circuit for short circuits to ground. If the output cannot be adjusted within the tolerances specified in this procedure, return the module to the factory for calibration.

Digital-to-Analog Converter Check and Adjustment

This procedure is performed to check and adjust the ladder network of the Type A604 Digital-to-Analog Converter modules. Use this procedure if the modules have been subjected to a drastic change in temperature or a mechanical shock sufficient to change the setting of the potentiometers. This test checks and aligns the ladder to compensate for variations in resistors of the divider network and for variations in the

output impedance of the level amplifiers. The ladder output voltage obtained only from the bit to be tested is compared with the output voltage resulting from all of the bits of lesser significance. The difference is trimmed so that it is equal to one least significant bit. This is accomplished by a test configuration which monitors the output of the modules at terminal PF11K on a high-gain ac-coupled oscilloscope, as the contents of the bit being adjusted and the complementary contents of all of the lesser significant bits are program alternated. All bits of greater significance are disabled by permanent test connections to simulate 0's, and the test is performed from the least significant to the most significant adjustable bits (from bit 5 to bit 0).

Perform the test as follows:

1. Connect the oscilloscope input to terminal PF11K, and adjust it for negative internal sweep triggering. Be sure the oscilloscope is solidly connected to the analog ground at terminal PF11F. The oscilloscope vertical preamplifier should be set to a sensitivity of approximately 2.5 mv/cm and calibrated with an external reference so that the least significant bit value of 2.4 mv can be readily observed.

2. Turn off all power in the PDP-8; remove the DAC module at location PF13; connect a FLIP CHIP module extender into the module connector at location PF13; insert the DAC module to the extender; and then restore PDP-8 power.

3. Connect the analog ground at terminal PE16EC to the DAC input terminals corresponding to bits 0 through 04 at terminals PF11U, PF11T, PF12U, PF12T, and PF13H.

4. Store the program listed in Table 9-6 in the PDP-8 core memory by means of the SWITCH REGISTER, LOAD ADD key, and DEP key. If this test is to be repeated periodically, the program can be punched on tape and stored by means of the Readin Mode Loader as described in Chapter 8 of this manual.

5. Start the program by loading the initial address into the PC by means of the SWITCH REGISTER and the LOAD ADD key.

6. Read and record the value of the two levels of the square wave displayed on the oscilloscope. The higher amplitude value corresponds to the condition when the bit being checked (bit 5) is a binary 1 and all less significant bits are 0's. The lower amplitude value corresponds to the condition when the bit being checked is a binary 0 and all less significant bits are 1's. Compare these two values, and adjust the potentiometer (R20 for bit 5) until the higher amplitude is 2.4 mv greater than the smaller

amplitude or until the higher amplitude is equal to the value listed in Table 9-5. During this adjustment it is possible to invert the relative values of the two signal amplitudes, so care should be taken to prevent adjustment so that the bit being checked is of lower value than the value of the less significant bits.

TABLE 9-6 DIGITAL-TO-ANALOG CONVERTER ADJUSTMENT PROGRAM

Address	Contents	Mnemonic	Comments
6000	7200	CLA	INITIALIZE
6001	1207	TAD PAD	FETCH PATTERN ADDRESS-1
6002	7001	IAC	CORRECT PATTERN ADDRESS
6003	3207	DCA	STORE CORRECTED PATTERN ADDRESS
6004	1607	TAD I PAD	LOAD APPROPRIATE PATTERN
6005	7040	CMA	COMPLEMENT PATTERN
6006	5205	JMP .-1	ALTERNATE PATTERN CONTINUOUSLY
PAD 6007	6007		PATTERN ADDRESS (PAD)
6010	0020		PATTERN BIT 7
6011	0040		PATTERN BIT 6
6012	0100		PATTERN BIT 5
6013	0200		PATTERN BIT 4
6014	0400		PATTERN BIT 3
6015	1000		PATTERN BIT 2
6016	2000		PATTERN BIT 1
6017	4000		PATTERN BIT 0

7. Stop the program by pressing the STOP key on the operator console.

8. Disconnect the ground connection from terminal PF13U made during step 3.

9. Check bit 4 by repeating steps 5 through 7 and adjusting potentiometer R10 of module PF13. Then disconnect the ground connection made to terminal PF12T during step 3.

10. Turn off power; remove the module extender from PF13; connect the module just checked in location PF13; remove the module from location PF12; insert the module extender in PF12; connect the removed module into the extenders; and restore computer power.

11. Check bit 3 by repeating steps 5 through 7 and adjusting potentiometer R20. Then disconnect the ground connection made to terminal PF12U during step 3.

12. Check bit 2 by repeating steps 5 through 7 and adjusting potentiometer R10 of the module at PF12. Then disconnect the ground connection made to terminal PF11T during step 3.

13. Turn off computer power; remove the module extender from location PF12; connect the module just checked into PF12; remove the module from PF11; insert the module extender into location PF11; connect the removed module into the extender; and restore computer power.

14. Check bit 1 by repeating steps 5 through 7 and adjusting potentiometer R20. Then disconnect the ground connection made to terminal PF11U during step 3.

15. Check bit 0 by repeating steps 5 through 7 and adjusting potentiometer R10 of the module at location PF11.

The 0 end point of the DAC network can be checked and adjusted as follows:

1. Load a word containing all 0's into any convenient core memory address by means of the SWITCH REGISTER, LOAD ADD key, and the DEP key. Then clear the accumulator by setting this word into the AC by means of the SWITCH REGISTER, LOAD ADD key, and the EXAM key.

2. Calibrate the oscilloscope so that analog ground can be determined by a fixed position on the graticule.

3. Connect the oscilloscope to the ladder output at terminal PF11K, and measure any voltage differential between the analog ground and the ladder output. Choose a bias resistor (wired from +10v to DAC OUTPUT) which causes the voltage difference read on the scope to approach 0 (0 ±1 mv).

The full-scale end point of the ladder network can be checked and adjusted as follows:

1. Load a word containing all binary 1's into the AC by using the keys and switches on the operator console as in step 1 of the previous procedure.

2. Connect the oscilloscope input to terminal PE16E, and adjust the position to some fixed measuring point on the graticule; then disconnect the oscilloscope from this point.

3. Connect the oscilloscope input to terminal PF11K and measure the output voltage of the ladder network. Adjust the output of the Type A704 Precision Power Supply module at location PF16 until the voltage obtained on the oscilloscope is exactly −10v minus the digital value of the least significant bit.

4. Remove all test connections, and restore all modules to their normal positions.

Since the two end-point adjustments interact, it is difficult to align them both perfectly while maintaining linearity. A more convenient method is to adjust the 0 and half-full scale points for optimum fit, which permits closer control over the lower weighted (and therefore more error sensitive) bits. The two end points can be checked and adjusted more accurately if the potentiometric voltmeter is substituted for the oscilloscope in the two preceding procedures. This method is recommended.

The Difference Amplifier Check and Adjustment

The Type A502 Difference Amplifier module at location PE11 should be tested periodically and at any time when it has undergone severe temperature change or mechanical shock. The need for readjustment depends upon the accuracy required and upon the environment. Adjustment of the common balance is made by turning potentiometer R5, and zero set is adjusted by means of potentiometer R8.

To perform the checks:

1. De-energize the PDP-8, remove the module from location PF11; insert a Type W380 FLIP CHIP Module Extender into connector PF11; insert the module into the extender; then energize the PDP-8.

2. Connect the two inputs of a dual-trace oscilloscope to the two output terminals PE11F and unground PE11V. Then connect the oscilloscope to this terminal of the difference amplifier. Connect the oscilloscope ground to the module ground at terminal PE16C.

3. Connect the difference amplifier input terminals PE11N and PE11P to an ungrounded sine wave source of approximately 10 mv amplitude, 30 to 1000 cps, and biased at −5v.

4. Connect the oscilloscope trigger input to one of the difference amplifier input terminals to synchronize the trace.

5. Observe that the two difference amplifier output signals displayed on the oscilloscope appear as two complementary square waves. Adjust the lower module potentiometer so that the output signal at terminal PE11V is symmetrical, and then adjust the upper module potentiometer until the output signal at terminal PE11F is symmetrical (these adjust- must be performed in the sequence given).

To improve the resolution of these adjustments, repeat the procedure with the sine wave input reduced to 5 mv. It may be necessary to repeat the adjustment sequence several times since there is interaction between the two potentiometers.

This concludes the maintenance of the Type 189 Analog-to-Digital Converter. De-energize the PDP-8, remove test connections, and restore the original connections and condition of the converter.

CORRECTIVE MAINTENANCE

The PDP-8 is constructed of highly reliable transistorized FLIP CHIP modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. Neither special test equipment nor tools are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6016 with a Type 131 Current Probe Amplifier is very helpful in monitoring memory currents. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-8. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

1. Preliminary investigation to gather all information and to determine the physical and electrical security of the computer.

2. System troubleshooting to locate the fault to within a module through the use of operator console troubleshooting, signal tracing, or aggravation techniques.

3. Circuit troubleshooting to locate defective parts within a module.

4. Repairs to replace or correct the cause of the malfunction.

5. Validation tests to ensure that the fault has been corrected.

6. Log entry to record pertinent data.

Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible data about the symptoms given when the fault occurred, such as the program in progress, condition of operator console indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the power supply checks as described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

System Troubleshooting

Do not attempt to troubleshoot the system without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation. Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to ensure that the PDP-8, and not the peripheral equipment, is actually at fault before continuing with corrective maintenance procedures. Faults in equipment which transmits or receives information or improper connection of the system frequently give indications similar to those caused by computer malfunction. Faulty ground connections between peripheral equipment and the computer are a common source of trouble. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

Maindec Diagnostic Programs

The Maindec diagnostic programs listed in Table 9-1 are provided for locating sources of malfunction within the processor, memory, and I/O equipment. Since these divisions encompass the complete PDP-8 system, any trouble can be located generally by the Maindec programs, and a local program loop may be devised to pinpoint the malfunction to a specific module.

Maindec 801, 802, and 803 specifically test processor and memory functions. Maindec 810, 812, and 814 test functioning of the I/O equipment. These diagnostic programs are particularly useful under marginal checking conditions.

Maindec 801 tests the instruction cycling, processor registers, and controls (including the PC). This program also tests the optional Extended Arithmetic Element Type 182 and Memory Extension Control Type 183. Maindec 801 is an exceptionally thorough test that provides detailed printouts or table look-up information to direct maintenance personnel to specific modules when it detects a fault condition. Therefore this program should be used as the basic troubleshooting tool for all but the most obvious faults. Maindec 802 tests memory core storage by producing bit patterns in the cores that will cause worse noise conditions within the core array. Defective cores are detected in this manner. Maindec 803 tests address selection, and is, therefore, a powerful means of troubleshooting the entire memory address system, including the MA register, MB register, memory selector switches, and all controls associated with these functions.

Each Maindec diagnostic program instruction manual contains full particulars for loading the program, interpreting the results, and operating the PDP-8 for diagnostic testing. Chapter 8 of this manual also contains instructions for loading and starting Maindec programs.

If maintenance personnel can isolate the fault to the computer but cannot immediately localize it to a specific logic function, it usually lies within either the core memory or the processor logic circuits. Proceed to the memory troubleshooting or logic troubleshooting procedures. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, employ an aggravation test to locate the source of the fault.

Memory Troubleshooting

If the entire memory system fails, use the multimeter to check the read/write and inhibit outputs of the Type 708 Power Supply. Measure the voltages as indicated in Table 9-3. Do not attempt to adjust this supply. If the supply is defective, troubleshoot it and correct the cause of the trouble; then adjust the output voltage by performing the memory current check. If the power supply is functioning properly, proceed as follows:

The following test setup causes the core memory to cycle continuously, selecting sequential addresses by advancing the contents of the MA for each cycle.

1. De-energize the computer.

2. Connect one jumper from terminal PB32U to ground, and connect another jumper from terminal PC20U to ground.

3. Restore computer power and press the START key.

This discussion references the X- and Y-axis selection drawings, BS-D-8M-0-12 and BS-D-8M-0-13 and the memory control drawing BS-D-8M-0-15. Look at the X- and Y-axis drawings, and note that a core address is selected by a combination of two Type G209 Memory Selectors--one on the left side of the array, the other on the bottom of the array. READ or WRITE transitions, buffered by the BD module at location MC16, trigger all Type G209 Selectors which generate and distribute the actual read/write current to specific address lines. In each axis, selection of the two Type G209 switches is accomplished by the bit configuration in the MA register. The actual read/write current pulses flow from the positive supply line, through a left Type G209 Selector, through a horizontal core matrix line, through the core and diodes, down a vertical core matrix line to a bottom Type G209 Selector, and into the negative return line.

With the MA register advancing sequentially, use an oscilloscope with current probe connected to any one of the left Type G209 terminals (M, H, N, J), connected in common to the 80-ohm limiting resistor, to measure all read/write current pulses for one axis of the complete core memory. The oscilloscope will show a train of current spikes and missing spikes represent malfunctioning addresses. Read currents are at terminals L and P; write currents are at terminals F and K of each drive selector. Before loading the Address Test Maindec program to find specific address malfunction, trace the read/write gating pulses from the BD module at MC16 and all the E and D terminals of every Type G209 module. A Type G209 Memory Selector module cannot select without the gating pulse. Monitor individual drive lines by putting the W025 Connector modules on two module extenders and clipping the current probe on the drive wire leading directly to the core array. If the read/write currents are not as specified on the memory array labels, adjust the Type G808 Power Supply Control module accordingly.

Perform the Memory Address Test program (Maindec 803) to locate defective core memory addresses. Complete the entire program and record all addresses which fail. inspect the record of failure addresses for common bits. Refer to engineering drawings BS-D-8M-0-12 and BS-D-8M-0-1, and check the memory selectors that decode common bits of the failing addresses. Also check the associated memory matrix module.

If an address is dropping bits, use the keys and switches of the operator console to deposit all binary 1's in that address. Then examine the contents of the address to determine which bit position is not being set (contains a 0). Check the sense amplifier, inhibit driver, and inhibit resistor for the associated bit. Also check the memory inhibit current as described in the memory current check.

If an address is picking up bits, use the operator console to deposit all binary 0's in that address, and proceed as described in the previous paragraph.

If bits are being picked up or dropped out at all addresses, adjust the slice level (R3) of the Type G008 Master Slice Control module at location MB31. If either the positive or negative output of several sense amplifiers is being clipped, adjust the second stage clamp potentiometer (R13) of the Type G008 module.

To locate the cause of a specific address failure, use the oscilloscope and current probe to trace read and write current while performing a repetitive routine such as the Memory Address Test program or the Memory Checkerboard Test program.

Perform the Memory Checkerboard Test program (Maindec 802) to troubleshoot all other memory conditions.

Logic Troubleshooting

If the instructions do not seem to be functioning properly, perform the Instruction Test program (Maindec 801). This test halts to indicate instructions that fail. When an instruction fails, as indicated by the operator console indicators when the program stops or by the diagnostic printout that follows the error halt, consult the descriptive manual for Maindec 801 to obtain an interpretation that will localize the fault to within two modules.

If the computer interrupt system or the Teletype teleprinter do not seem to be functioning properly, perform the Teleprinter Test program (Maindec 814). If the Teletype tape reader or punch operation is questionable, perform the Read Paper Tape Test (Maindec 810) or the Punch Paper Tape Test (Maindec 812). Refer to the Teletype documents for detailed maintenance information on the Model 33-ASR Set.

Signal Tracing

If the fault has been located within a functional logic element, program the computer to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control signals or clock pulses, which are available on individual module terminals at the wiring side of the equipment. Circuits transferring signals with external equipment are most likely to encounter difficulty. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal-tracing method is useful to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. If an intermittent malfunction occurs, combine signal tracing with an appropriate form of aggravation test.

Aggravation Tests

Trace intermittent faults through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

To reveal intermittent failures caused by poor wiring connections, vibrate modules while running a repetitive test program. Often, tapping a wooden rod held against the handles of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the downtime limitations of equipment use. Where downtime must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module, power supply, or standard component which can be inserted into the system when troubleshooting procedures have traced the fault to a particular component. Return of the module to the factory for repairs, or static and dynamic bench tests can then be performed without interfering with system operation. Where downtime is not critical, the spare parts list can be reduced and module troubleshooting procedures can be performed with the modules in-line (within the system). Although in-line module troubleshooting extends the downtime of the system, it is economical of personnel time because the module can be program exercised to locate the cause of the fault more rapidly.

Module Circuits

Formal engineering schematic diagrams of each module are supplied with each PDP-8 system and should be referred to for detailed circuit information. Copies of the engineering schematic diagram for unusual modules or modules not described in the Digital FLIP CHIP Modules Catalog are presented in Chapter 10 of this manual. The basic function and specifications for standard modules are presented in the Digital FLIP CHIP Modules Catalog, C-105. The following design considerations may also be helpful in troubleshooting such standard modules:

1. Forward-biased silicon diodes are used in the same manner as Zener diodes, usually to provide a voltage differential of 0.75v. For instance, a series string of four diodes produces the −3 vdc clamp voltage used in most modules.

2. An incoming pulse which turns off the conducting transistor amplifier changes the state of DEC flip-flops. Since these flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

3. Fixed-length delay lines such as the W300 are extremely reliable and very seldom malfunction. However, if a malfunction should occur, do not replace these delay lines on the printed-wiring board. In such cases return the entire module to DEC for repair.

4. The W607 and W640 modules both contain three independent pulse amplifiers. The time required to saturate the interstage coupling transformer determines output pulse duration. No multivibrators or other RC timing circuits are used in these pulse amplifiers.

In-Line Dynamic Tests

To troubleshoot a module while maintaining its connection within the system:

1. De-energize the computer.

2. Remove the suspect module from the mounting panel.

3. Insert a W980 FLIP CHIP Module Extender into the mounting panel connector which normally holds the suspect module.

4. Insert the suspect module into the module extender. All components and wiring points of the module are now accessible.

5. Energize the computer and establish the program conditions desired for troubleshooting the module. Trace voltages or signals through the module, using a dc voltmeter or an oscilloscope, until the source of the fault is located.

In-Line Marginal Checks

Marginal checks of individual modules can be performed within the computer to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module mounting panel by the normal marginal-checking method. Perform these checks with the aid of a modified W980 FLIP CHIP Module Extender. To modify an extender for these checks:

1. Disconnect module receptacle terminals A, B, and C from the male plug connection terminals by cutting the printed wiring for these lines near the plug end and removing a segment of this wiring in each line.

2. Solder a 3-ft test lead to the printed wiring for terminals A, B, and C. Make this solder joint close to the receptacle end of the extender, certainly on the receptacle

side of the wiring break. Observe the normal precautions when making this connection to ensure that excessive heat does not delaminate the printed-wiring board and that neither solder nor flux provides conduction between lines.

3. Attach a spade lug, such as an AMP 42025-1 Power Connector to the end of each test lead and label each lead to correspond to the A, B, or C terminal of the receptacle to which it is connected.

To marginal check a module within the computer:

1. De-energize the computer.

2. Remove the module to be checked from the module mounting panel, replace it with the modified extender, and insert the module in the extender.

3. If performing the +10 marginal check, connect test lead A to the +10 MC orange connector terminal at the bottom of the cabinet doors. Connect test lead B to the normal −15v blue connector terminal and test lead C to GND. Keep all SPDT normal/marginal switches in the down position. If performing the −15 marginal check, connect test lead A to the normal +10v red connector, test lead B to the −15 MC green connector terminal, and test lead C to GND. Keep all SPDT normal/marginal switches in the down position.

4. Restore computer power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer are useful as a guide to marginal checking modules.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and is often helpful in tracing the cause of a fault to a particular component part.

6. Repeat steps 3, 4, and 5 for both bias voltages. If margins are ±5v on the +10 vdc supplies and the −15 vdc supply can be adjusted between −12 and −15v without module failure, assume that the module is operating satisfactorily. If the module fails before reaching these margins, use normal signal-tracing techniques within the module to locate the source of the fault.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between the collector and the emitter or an open circuit in the base-emitter path cause most catastrophic failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. To obtain a more reliable indication of diode or transistor malfunction use one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range, and connect it across the suspected connection. Poke at the wires or components around the connection or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Detect current interruptions of very short duration, caused by an intermittent connection, by connecting a 1.5v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope, while probing the connection.

Dynamic Bench Tests

In general, return a module to DEC for repair or replacement if it fails marginal in-line tests or is suspect for other reasons. Many modules require special equipment for dynamic testing, since the timing of pulse amplifiers and delay modules must be rigorously maintained within narrow limits. Dynamic tests, therefore, should be oriented only toward discovery of defective semiconductors. Dynamic tests may be performed with a Type H901 Patchcord Mounting Panel connected to the computer power supply outputs by Type 914 Power Jumpers. Then apply simulated ground-level signals to the module under test, using Type 911 Patchcords. An oscilloscope connected to terminals on the front of the Type H901 panel can monitor output terminals of the module under test. (Simulated negative-level signal inputs are not required, since FLIP CHIP module input terminals are internally clamped at −3v, so open input terminals simulate a −3v signal input.)

Repair

Limit repairs to FLIP CHIP modules to the replacement of semiconductors. In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, metallic rectifiers, or integrated circuits) which may be damaged by heat, take the following special precautions:

1. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

2. Use a 6v soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

3. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When removing any part of the equipment for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or better quality and equal or narrower tolerance.

Spare Parts

Each user of the PDP-8 system should establish a spare parts stock in accordance with the extent of the available repair facilities. The following considerations are helpful in determining what spare parts should be stocked.

Teletype

Users who do not have maintenance personnel trained in the maintenance and repair of Teletype units should keep a complete Model 33 Automatic Send Receive Teletype near the computer. If the on-line unit becomes defective, substitute the spare to avoid computer downtime. However, many users have facilities for the maintenance of Teletype units, in which case it is suggested that spare parts be stocked as listed in Table 9-7 and that one of each Teletype maintenance tool listed in Table 9-8 be stocked. All of these items can be obtained from the Digital Equipment Corporation or from the Teletype Corporation.

TABLE 9-7 SPARE PARTS FOR PRINTED KEYBOARD-MODEL ASR 33

Quantity	Item	Part No.	Quantity	Item	Part No.
1	Circuit board	181821	1	Power pack assembly	182104
2	Tape fee sprocket	183071	1	Belt driven gear	181420
2	Lever, universal	180086	1	Drive gear	181411
1	Fuse (3.2 amp)	120167	1	Belt	181409
2	Distributor brush	180979	1	Shaft	181007
1	Dust cover	183067	2	Bearing	181002
1	Dust cover spring	183068			

TABLE 9-8 TELETYPE MAINTENANCE TOOLS

Item	Part No.	Item	Part No.
8-oz scale	110443	Handwheel	161430
32-oz scale	110444	Contact adjustment tool	172060
64-oz scale	82711	Gauge	180587
Set of gauges	117781	Gauge	180588
Offset screwdriver	94644	Bending tool	180993
Offset screwdriver	94645	Gauge	183103
8 crochet hook	151952	Extractor	182697
12 crochet hook	151959	Tweezer	151392

TABLE 9-8 TELETYPE MAINTENANCE TOOLS (continued)

Item	Part No.	Item	Part No.
Spring hook push	142555	Tommy wrench	6617
Spring hook pull	142554	Tommy wrench	73404
Screw holder	151384	Key level remover	151383
Handwheel adapter	181465		

Modules and Components

All of the module types used in the basic PDP-8 and in the prewired options are listed in Table 9-9. It is suggested that one module of each type be stocked as a spare part, except for the Type S111 and Type S603 modules for which the suggested quantity is three and two, respectively. If modules are to be repaired at the installation site, reduce this list of spare modules and stock the components listed in Table 9-10. The spare parts listed in Table 9-11 should be made available at each installation. All of the spare parts listed in this table are available from Digital Equipment Corporation. Note that S series modules are R series modules which have been specially adapted for use in the PDP-8. Usually this adaptation changes the value of clamped load resistors from 7.5K to 3.0K; so the output current is reduced by approximately 2 ma, and output waveforms have faster rise and fall times.

TABLE 9-9 MODULE LIST

Name	Type	Name	Type
	Basic PDP-8		
Inverter	B104	Diode Cluster	R002
Four Flip-Flops	B204	NAND Gate	R121
Delay with Pulse Amplifier	B360	PDP-8 Accumulator	R210
10 MC Pulse Amplifier	B602	MA, MB, PC	R211
DC Sense Amplifier	G007	3-Bit Shift Register	R220
Master Slice Control	G008	Delay	R302
Inhibit Driver	G208	Clock	R401
Memory Selector	G209	Crystal Clock	R405
Memory Selector Matrix	G608	Bus Driver	R650
Control for 708 Power Supply	G808	Inverter	S107
−15v Sense and Relay Driver	G809	Diode Gate	S111

*See S Series Modules at the end of Chapter 10.

TABLE 9-9 MODULE LIST (continued)

Name	Type	Name	Type
	Basic PDP-8 (continued)		
Binary-to-Octal Decoder	S151	Clamped Load	W005
DC Carry Chain	S181	Indicator Driver	W050
Dual Flip-Flop	S202	Teletype Connector	W070
Triple Flip-Flop	S203	Delay Line	W300
Dual Flip-Flop	S205	Schmitt Trigger	W501
Quadraflop	S284	Pulse Amplifier	W607
Pulse Amplifier	S602	Pulse Amplifier	W640
Pulse Amplifier	S603		
	Automatic Restart Type KR01		
*Diode Network	R002	*Pulse Amplifier	S602
*Delay	R302	*Schmitt Trigger	W501
*Inverter	S107		
	Extended Arithmetic Element Type 182		
*Diode Cluster	R002	*Diode Gate	S111
Diode Gate	R123	*Triple Flip-Flop	S203
MQ Register	R212	*Dual Flip-Flop	S205
*Crystal Clock	R405	*Pulse Amplifier	S602
*Inverter	S107	*Pulse Amplifier	S603
	Memory Extension Control Type 183		
Two Bus Drivers	B684	*Binary-to-Octal Decoder	S151
*Diode Cluster	R002	*Triple Flip-Flop	S203
Diode Gate	R123	*Dual Flip-Flop	S205
Flip-Flop	R201	*Pulse Amplifier	S603
*Inverter	S107	*Pulse Amplifier	W640
*Diode Gate	S111		
	Memory Parity Type 188		
*Inverter	B104	*Diode Cluster	R002
3-Bit Parity Circuit	B130	*Diode Gate	S111

*These modules are contained in the basic PDP-8 so duplicate spare modules are not required.

TABLE 9-9 MODULE LIST (continued)

Name	Type	Name	Type
	Memory Parity Type 188 (continued)		
*Delay with Pulse Amplifier	B360	*Dual Flip-Flop	S202
*DC Sense Amplifier	G007	*Pulse Amplifier	S603
*Inhibit Driver	G208		
	Analog-to-Digital Converter Type 189		
Difference Amplifier	A502	*Delay	R302
3-Bit DAC	A601	*Clock	R401
2-Bit DAC	A604	*Diode Gate	S111
−10v Precision Power Supply	A704	*Triple Flip-Flop	S203
Diode Gate	R123	*Pulse Amplifier	S603
	Data Line Interface Type 681		
*Diode Network	R002	*Inverter	S107
Diode Gate	R113	*Diode Gate	S111
*NAND Gate	R121	*Pulse Amplifier	S603
Diode Gate	R123		

*These modules are contained in the basic PDP-8 so duplicate spare modules are not required.

TABLE 9-10 SUGGESTED SPARE MODULE COMPONENTS

Quantity	Type	Quantity	Type
	Transistors		
5	DEC3009	1	2N1309
1	16J1	1	DEC2219
4	MM999	15	DEC28941A
1	SDA5	1	DEC28942A
1 SDA	SDA6	3	DEC28943B
1	2N215	1	2N2904
1	2N398A	10	2N3639
1	2N1184B	4	DEC1008
1	2N1305		

TABLE 9-10 SUGGESTED SPARE MODULE COMPONENTS (continued)

Quantity	Type	Quantity	Type
	Diodes		
1	D003	10	D670
1	D007	1	1N748
1	320A	1	1N750A
15	D662	1	1N758A
30	D664	*1	1N3208
	Pulse Transformers		
1	2046	5	2052
3	2051	1	2054

*Located in Type 708 Power Supply

TABLE 9-11 MISCELLANEOUS SPARE PARTS

Quantity	Item	Part No.
4	Rocker switch	74-RS-26-1-FB
2	Rocker switch	74-RS-9
2	Marginal switch	34-SS-26-1
*4	Rocker handles	74-4531
6	Indicator bulb	1762F
1	Fan	Howard 80-15
1	Relay	12-KRP-14DG
1	Power lock switch	34-4235

*Two brown and two white handles are suggested. This one part number applies to both colors, so color and part number must be specified on order.

Validation Test

Following the replacement of any electrical component of the equipment, perform a test to assure correction of the fault condition and to make any adjustments of timing or signal levels affected by the replacement. Take the test from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor has been replaced in a section of the Type 708 Power Supply, repeat the ripple check for that section as specified under Power Supply

Checks. If repairs or replacements are made in an area which is not checked during preventive maintenance, run the appropriate diagnostic program (Maindec) or devise an appropriate operational test. For example, if a flip-flop is repaired or replaced, completely check the register or control function performed by the flip-flop by manual setting and clearing, by improvised programmed exercise of the function, or by performance of the appropriate diagnostic program.

When time permits, perform the entire preventive maintenance task as a validation test. The reasons for this are:

1. If one fault has been detected and corrected, other components may be marginal.

2. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

CHAPTER 10

ENGINEERING DRAWINGS

This chapter contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct. The Table of Contents contains a complete listing of the drawings in this chapter.

DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the size of the original drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram
CD, cable diagram
CL, cable list
CS, circuit schematic
FD, flow diagram
PW, power wiring
RS, replacement schematic
UML, utilization module list
WD, wiring diagram
WL, wiring list

CIRCUIT SYMBOLS

Block schematic engineering drawings of DEC equipment indicate signal flow, logical functions, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using symbols that define the circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure 10-1 illustrates some of the symbols used in DEC engineering drawings.

LOGIC SIGNAL SYMBOLS

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

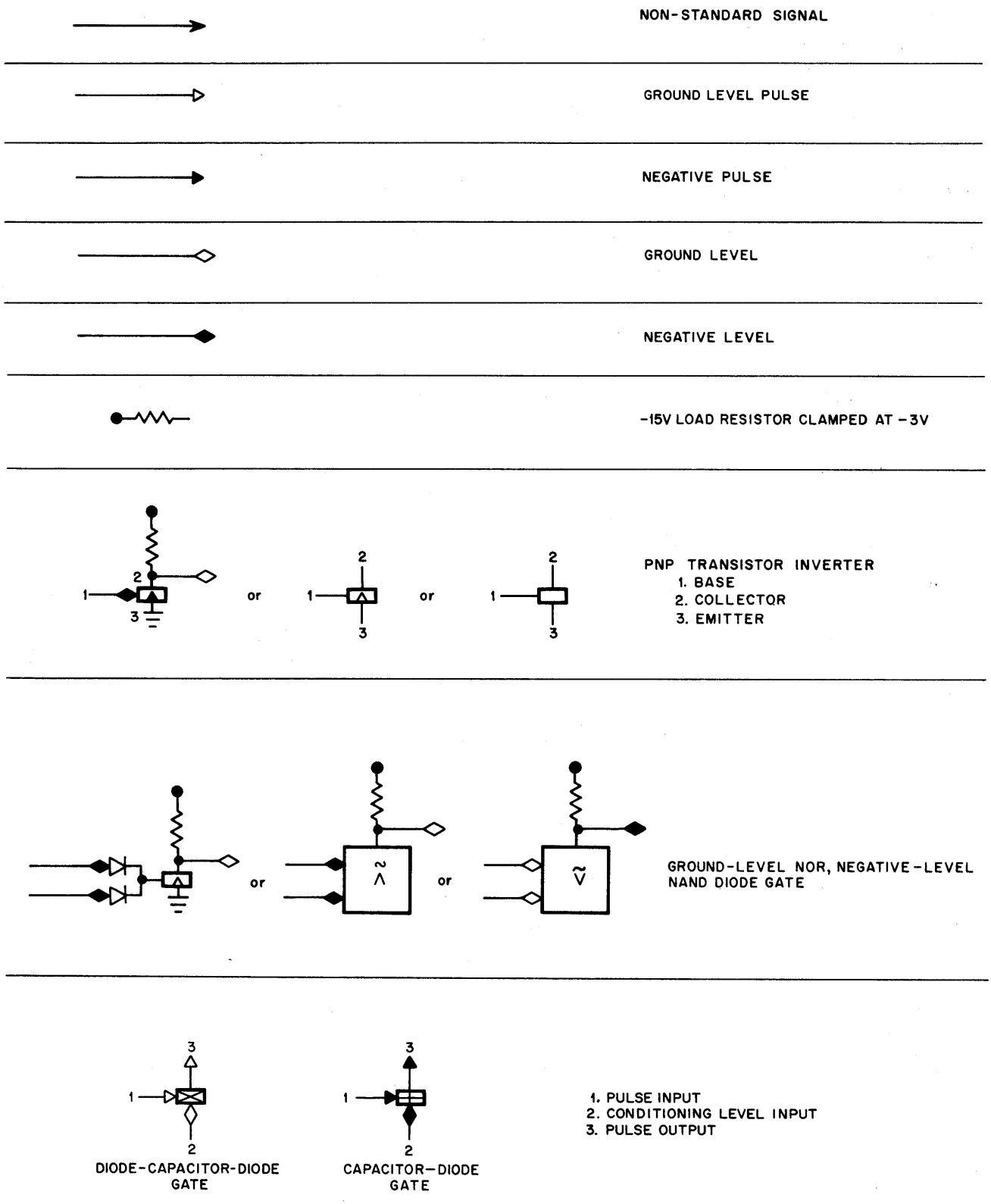
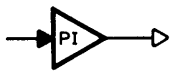
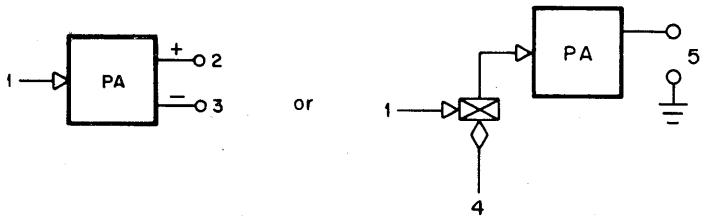


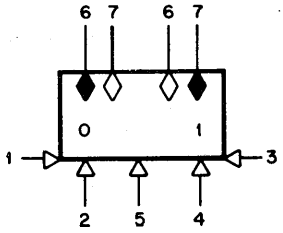
Figure 10-1 DEC Symbols



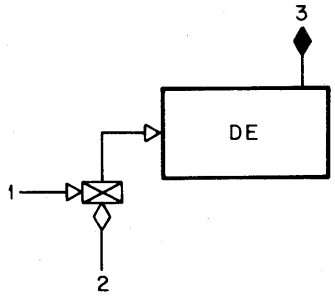
PULSE INVERTER



PULSE AMPLIFIER
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED
4. CONDITIONING LEVEL INPUT
5. DIRECT-COUPLED OUTPUT PULSE



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1



DELAY (ONE-SHOT MULTIVIBRATOR)
1. INPUT TRIGGER PULSE
2. INPUT CONDITIONING LEVEL
3. OUTPUT LEVEL, -3V DURING DELAY

Figure 10-1 DEC Symbols (continued)

Logic Levels

The standard DEC logic level is either at ground (0 to −0.3v) or at −3v (−2.5 to −3.5v). Logic signals generally have mnemonic names which indicate the assertion condition of the signal. An open diamond (——◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is also a DEC logic level and that −3v represents assertion. All logic signals at the conditioning level inputs of diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse will trigger operation of the gate.

Standard Pulses

DEC standard pulses are 2.5v in amplitude with reference to either ground or −3v, depending upon the type of module used. The width of standard pulses is either 40, 70, or 400 nsec as required for specific circuit configurations. The standard 2.5v negative pulse (−2.3 to −3.5v) is indicated by a solid triangle (——▶) and is always referenced with respect to ground, as shown in Figure 10-2.

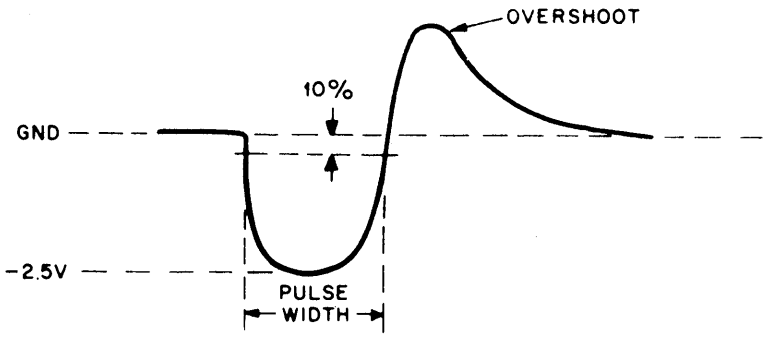


Figure 10-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle (——▷). The positive pulse goes either from −3v to ground or goes from ground to +2.5v (+2.3 to +3.0v).

FLIP CHIP Standard Pulses

FLIP CHIP circuit operation utilizes two types of pulses, R- and S-series and B-series. The pulse produced by R- and S-series modules starts at −3v, goes to ground (−0.2v) for 100 nsec, then returns to −3v. This pulse is shown in Figure 10-3.

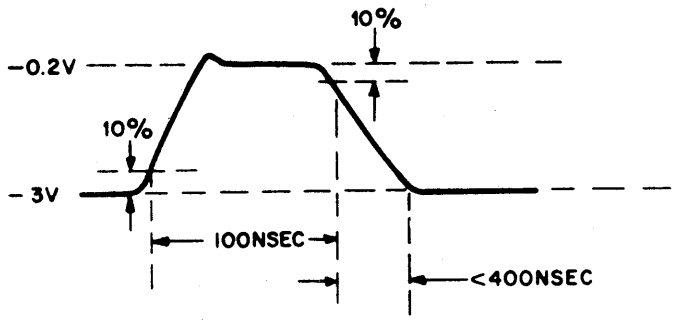


Figure 10-3 FLIP CHIP R- and S-Series Pulses

The B-series negative pulse is 2.5v in amplitude and 40 nsec in duration and is similar to the one shown in Figure 10-2. If this pulse arrives at the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series negative pulse.

Level Transitions

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) indicates this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (−3v to ground) or the negative (ground to −3v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level or is opposite that of the triangle to indicate triggering on the trailing edge. An arrowhead (——►) pointing in the direction of signal flow indicates nonstandard signals (power supply outputs, analog signals, etc.).

SEMICONDUCTOR SUBSTITUTION

Standard EIA components as specified in Table 10-1 can replace most DEC semiconductors used in modules of the PDP-8. Exact replacement is recommended for semiconductors not listed.

TABLE 10-1 SEMICONDUCTOR SUBSTITUTION

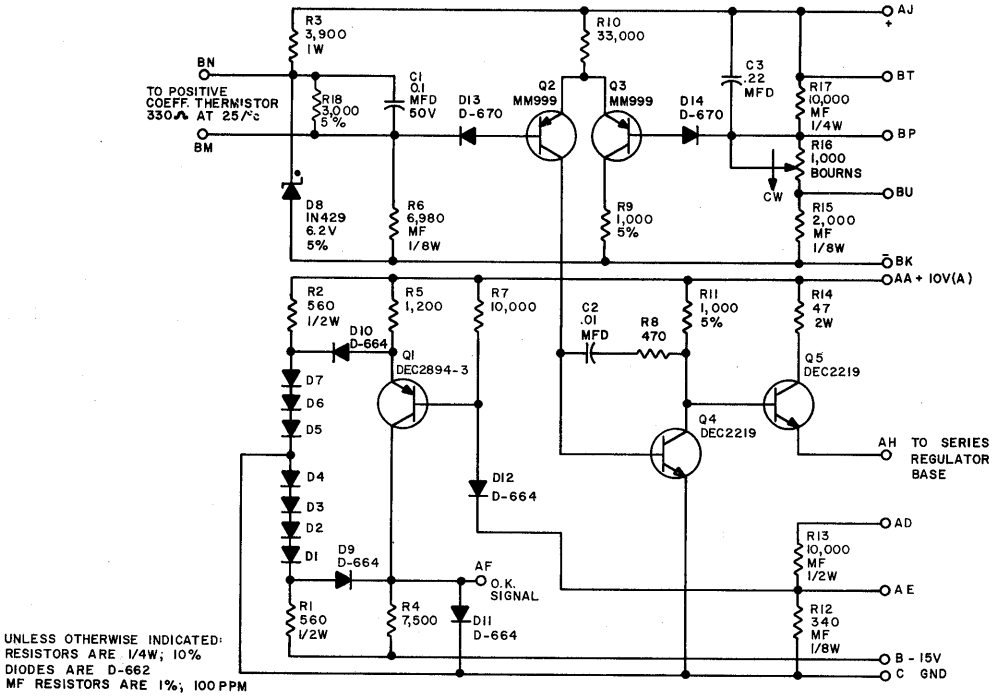
DEC	EIA	DEC	EIA
D-662	1N645	DEC 3639	2N3639
D-664	1N3606	DEC 3639-2	2N3639-2
D-670	1N3653	SDA-6	2N2060
D-668	two 1N3606 in series	1N429	1N429 6.2v 5%
DEC 1008	MM1008	1N449	1N449 6.2v 5%
DEC 2904	2N1132	1N762	1N762 5.5v 250 ohms 5%
DEC 3009	2N3009		

S SERIES MODULES

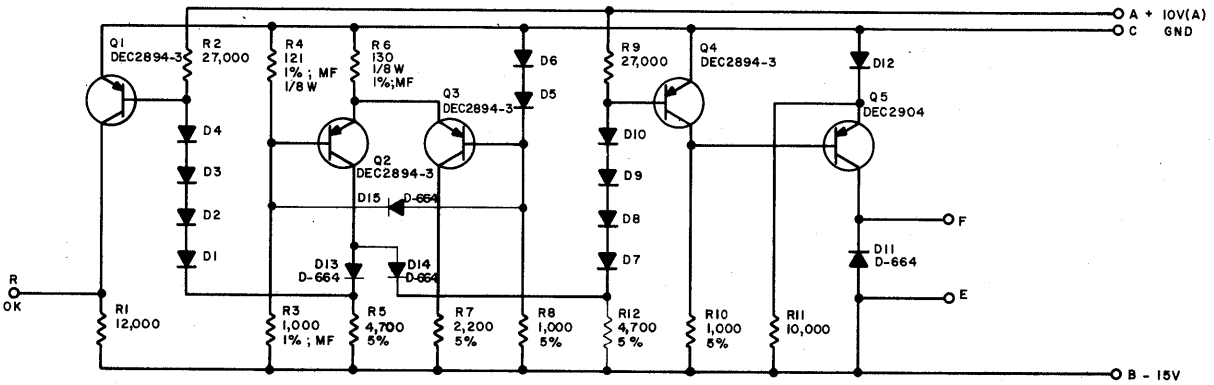
Ten R-series modules have been especially adapted for use in the PDP-8. The type numbers are the same, except that the prefix letter is S instead of R. They are:

S107	Inverter	S203	Triple Flip-Flop
S111	Diode Gate	S205	Dual Flip-Flop
S151	Binary-to-Octal Decoder	S284	Quadraflop
S181	DC Carry Chain	S602	Pulse Amplifier
S202	Dual Flip-Flop	S603	Pulse Amplifier

The S-series modules have 5-ma clamped loads instead of 2 ma. Their R-series counterparts may be modified by changing the load resistors to 3K ohms, but beware of decreased output drive.

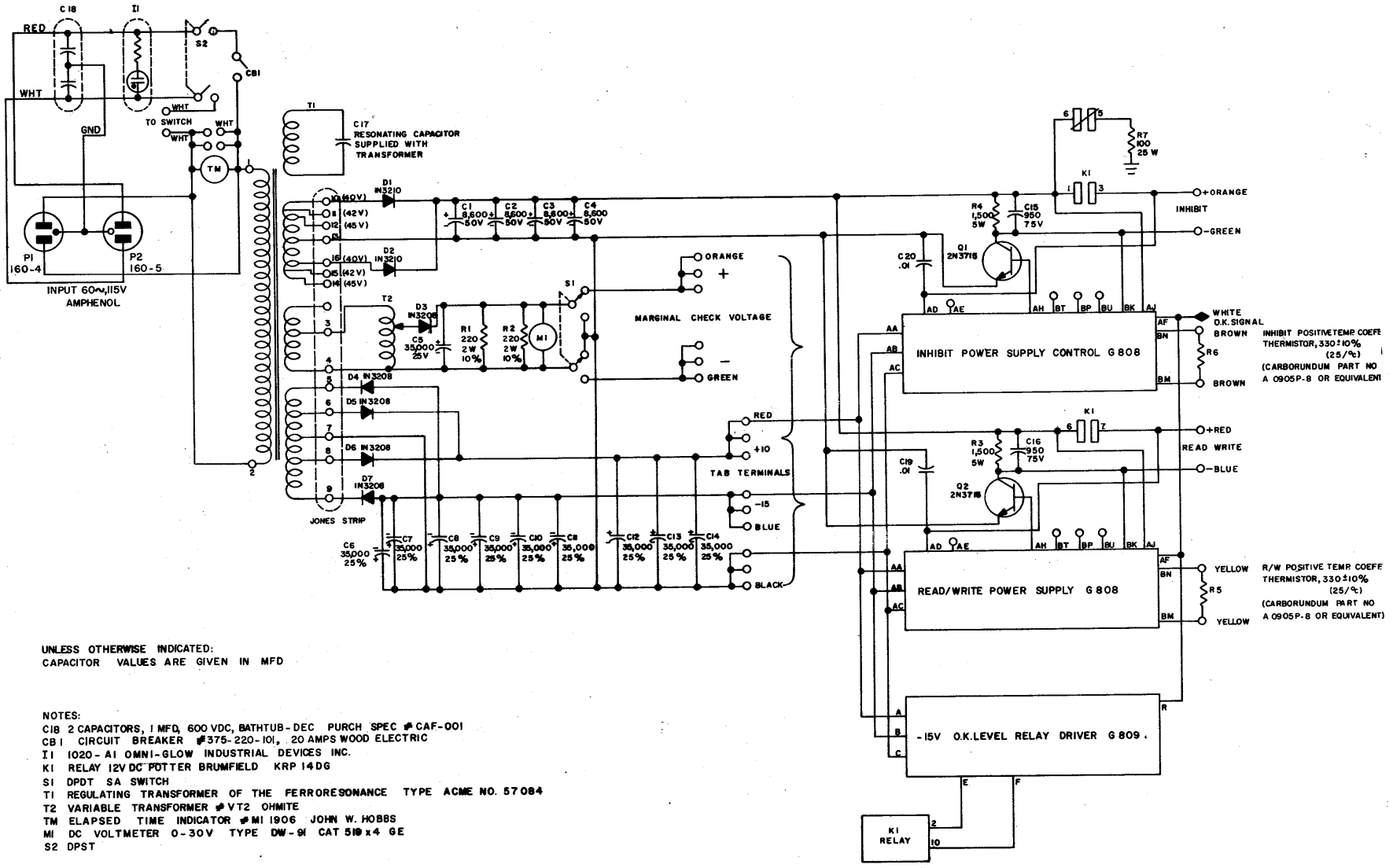


RS-B-G808 Control for 708 Power Supply



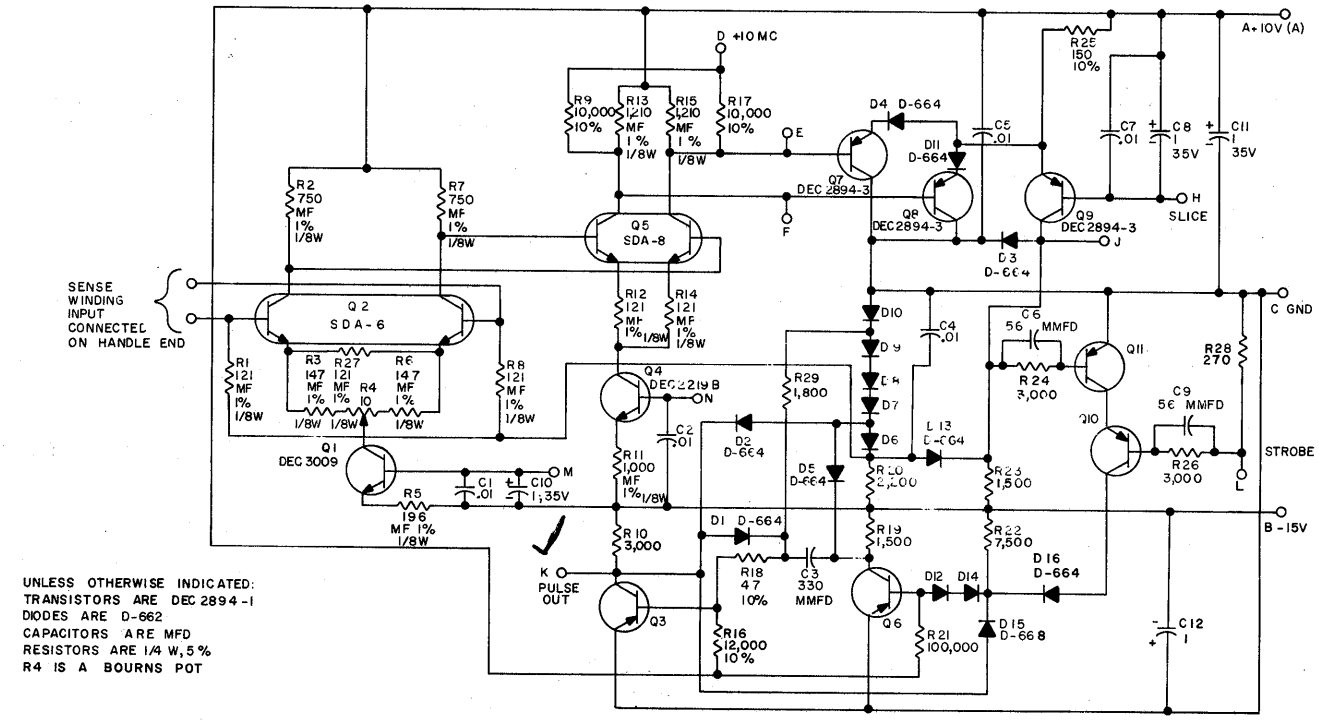
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-662

RS-B-G809 −15v Sense and Relay Driver

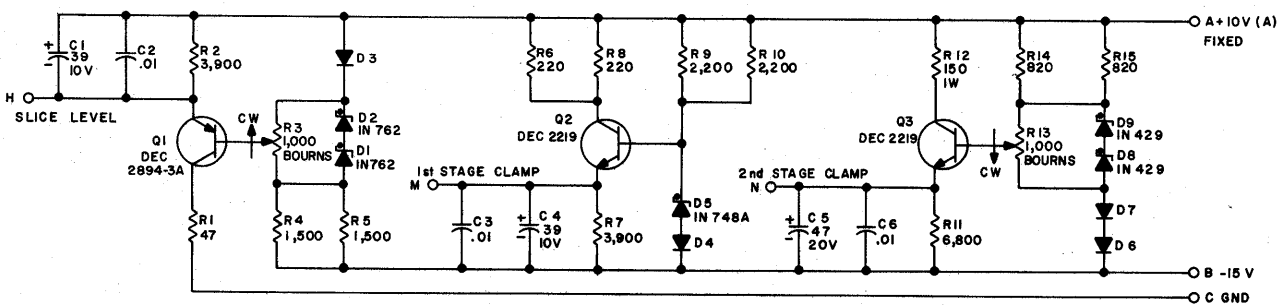


UNLESS OTHERWISE INDICATED:
CAPACITOR VALUES ARE GIVEN IN MFD

NOTES:
C18 2 CAPACITORS, 1 MFD, 600 VDC, BATHTUB-DEC PURCH SPEC # CAF-001
CB1 CIRCUIT BREAKER #375-220-101, 20 AMPS WOOD ELECTRIC
I1 1020-A1 OMNI-GLOW INDUSTRIAL DEVICES INC.
K1 RELAY 12V DC POTTER BRUMFIELD KRP 14DG
S1 DPDT SA SWITCH
T1 REGULATING TRANSFORMER OF THE FERRORESONANCE TYPE ACME NO. 57084
T2 VARIABLE TRANSFORMER # VT2 OHMITE
TM ELAPSED TIME INDICATOR # MI 1906 JOHN W. HOBBS
M1 DC VOLTMETER 0-30V TYPE DW-91 CAT 519x4 GE
S2 DPST

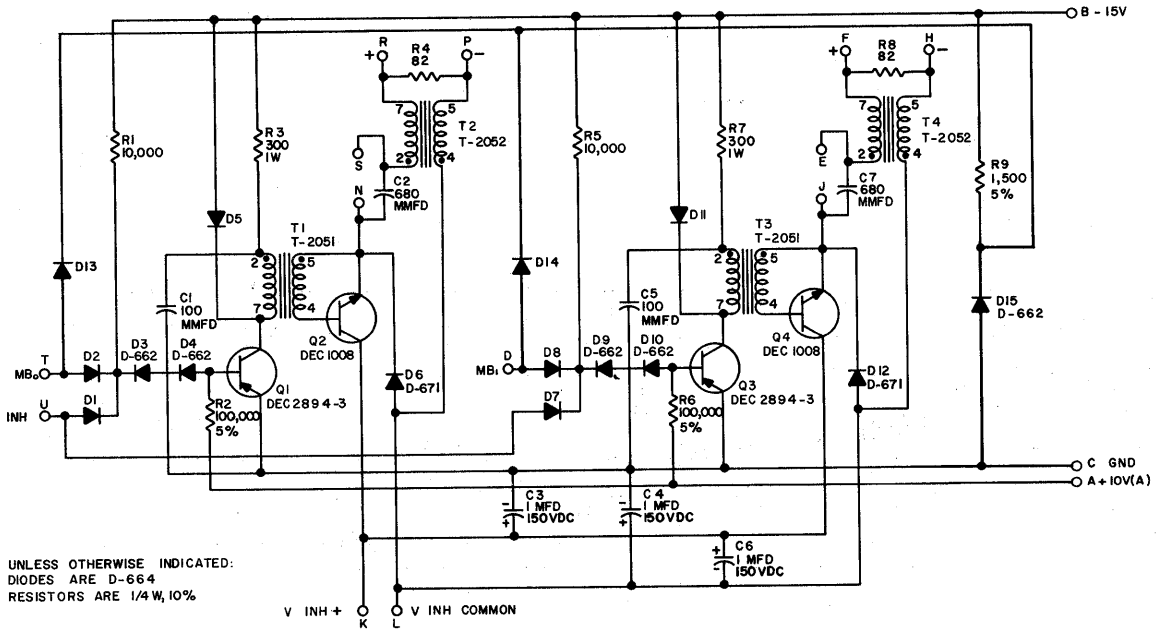


RS-B-G007 Sense Amplifier

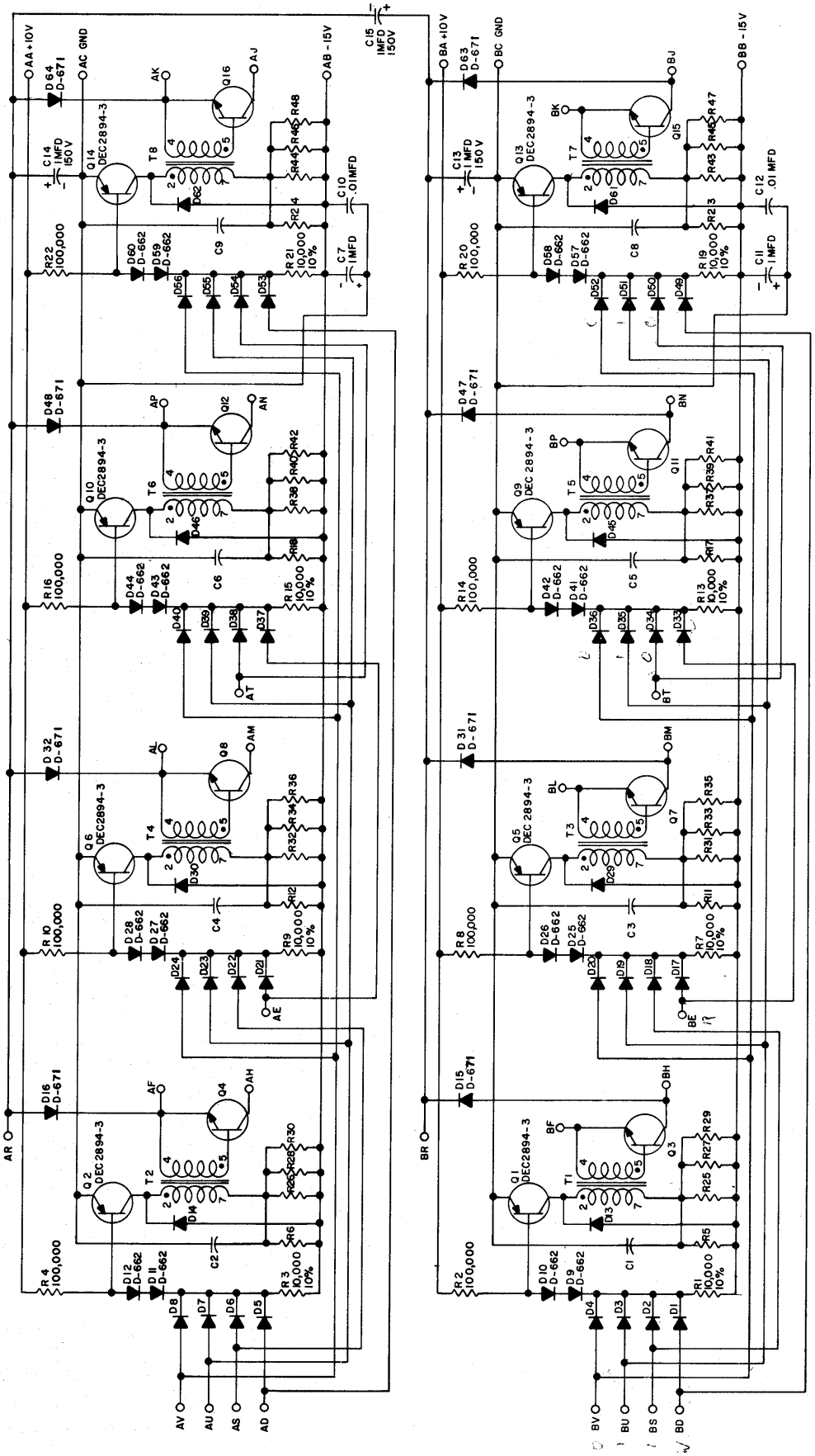


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE MFD
DIODES ARE D-662

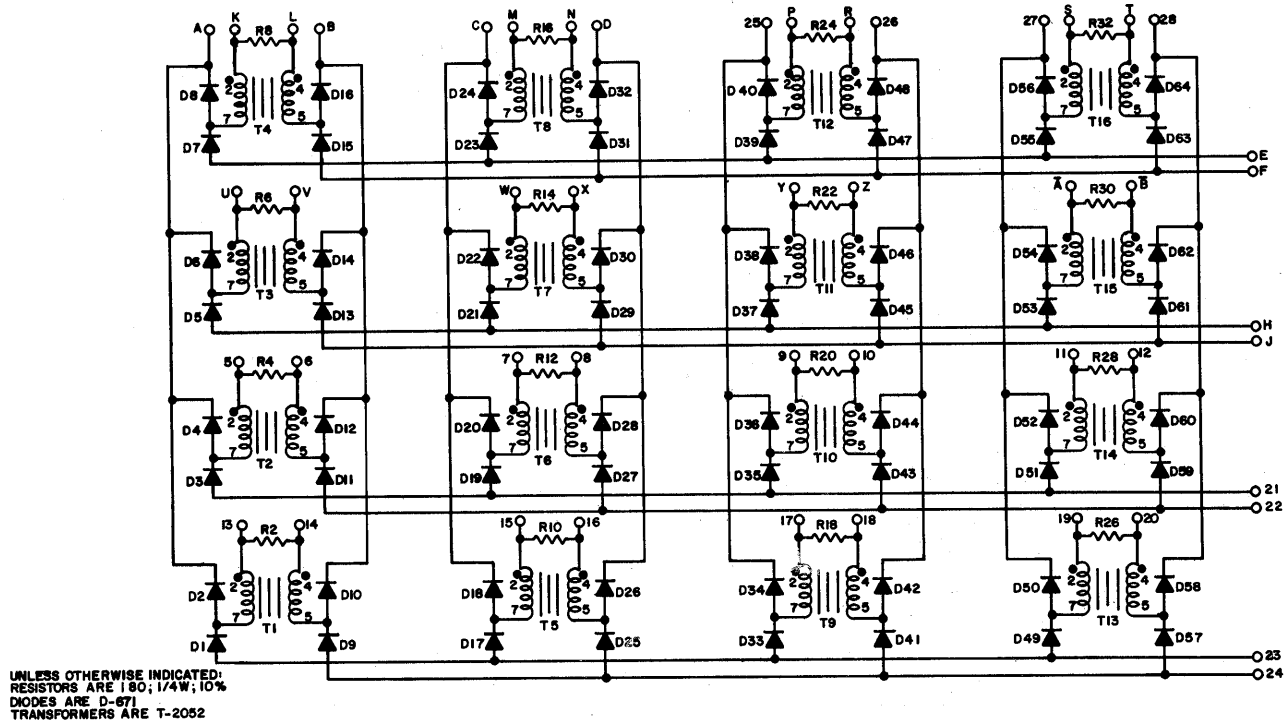
RS-B-G008 Master Slice Control



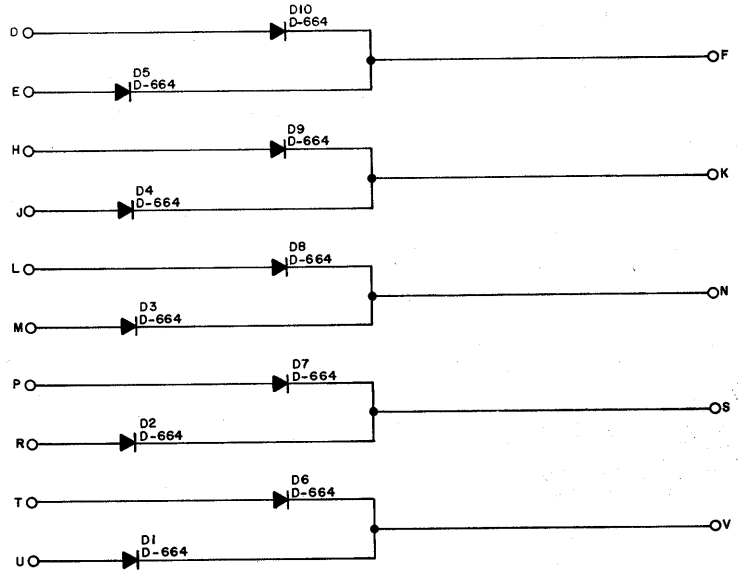
RS-B-G208 Inhibit Driver.



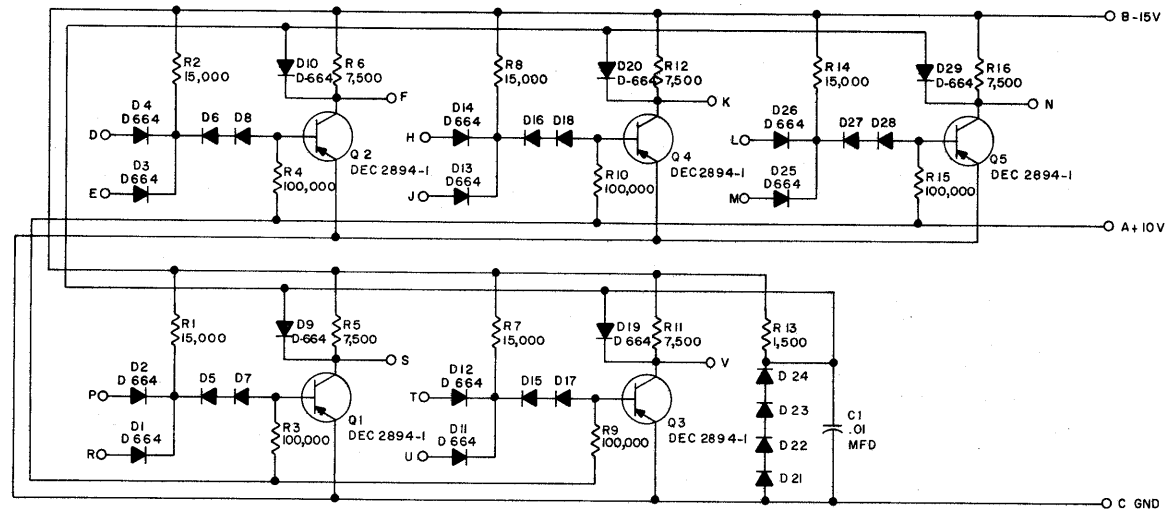
RS-C-G209 Memory Selector



RS-B-G603 Memory Selector Matrix

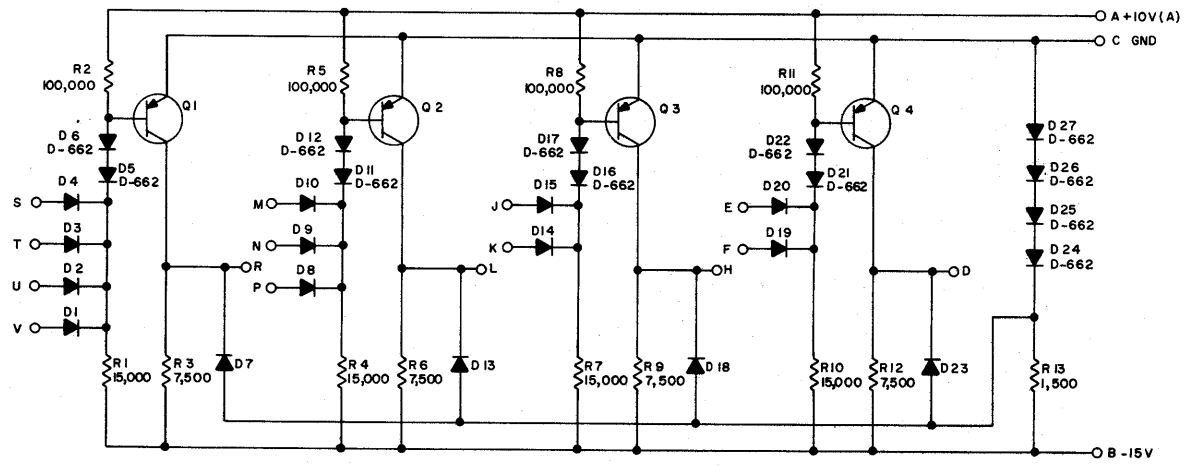


RS-B-R002 Diode Cluster



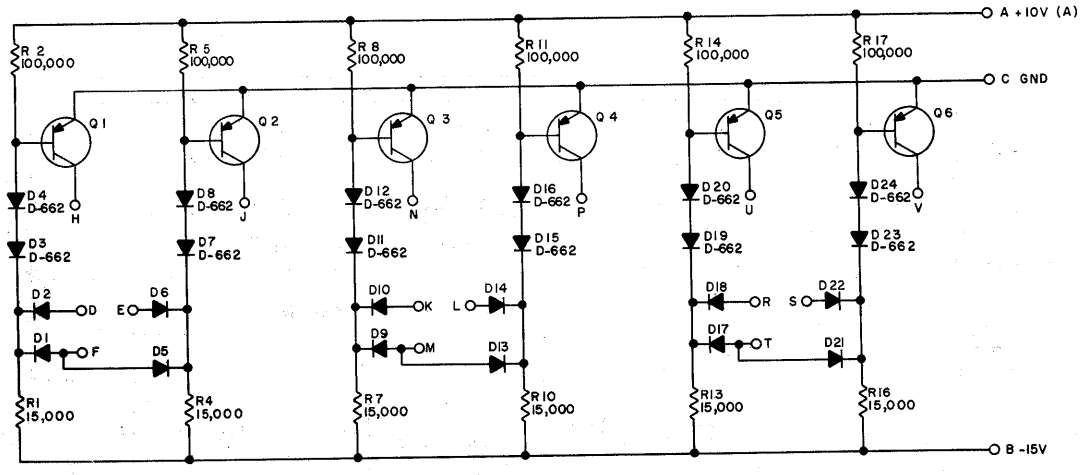
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

RS-B-R113 Diode Gate



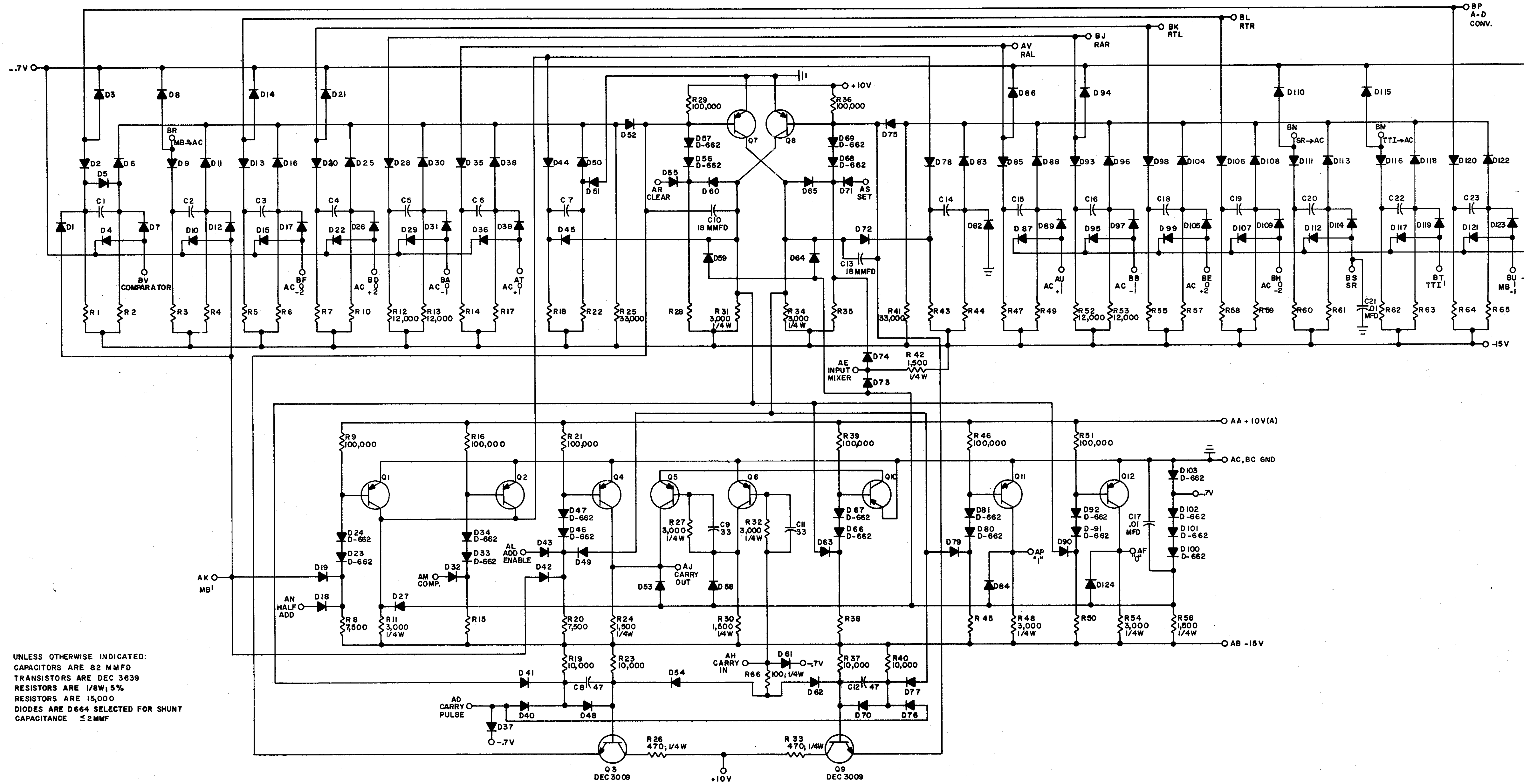
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
DIODES ARE D-664
RESISTORS ARE 1/4 W, 5%

RS-B-R121 NAND Gate



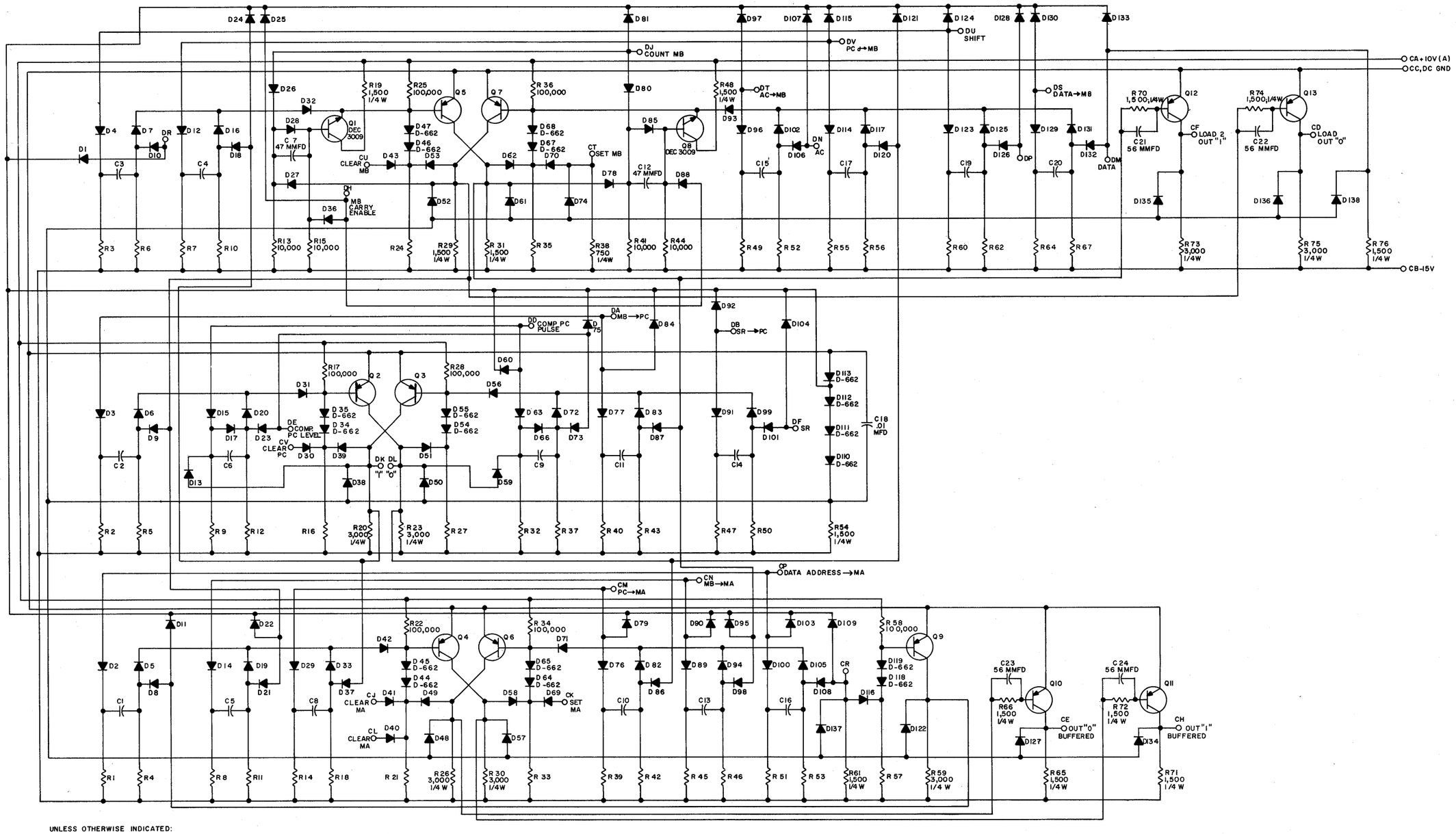
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639-0
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

RS-B-R123 Diode Gate



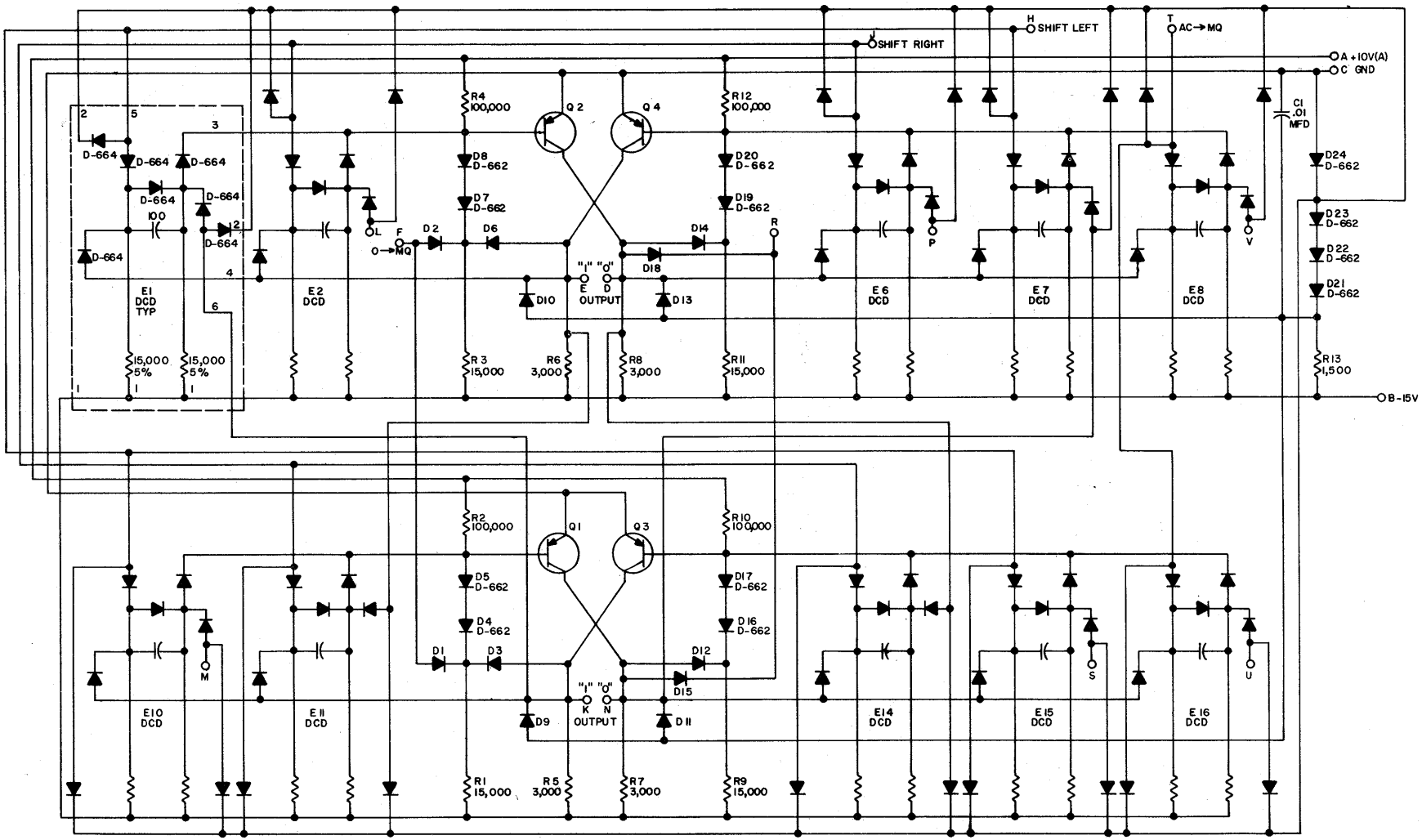
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 82 MMFD
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/8W; 5%
RESISTORS ARE 15,000
DIODES ARE D664 SELECTED FOR SHUNT CAPACITANCE ≤ 2 MMF

RS-D-R210 PDP-8 Accumulator

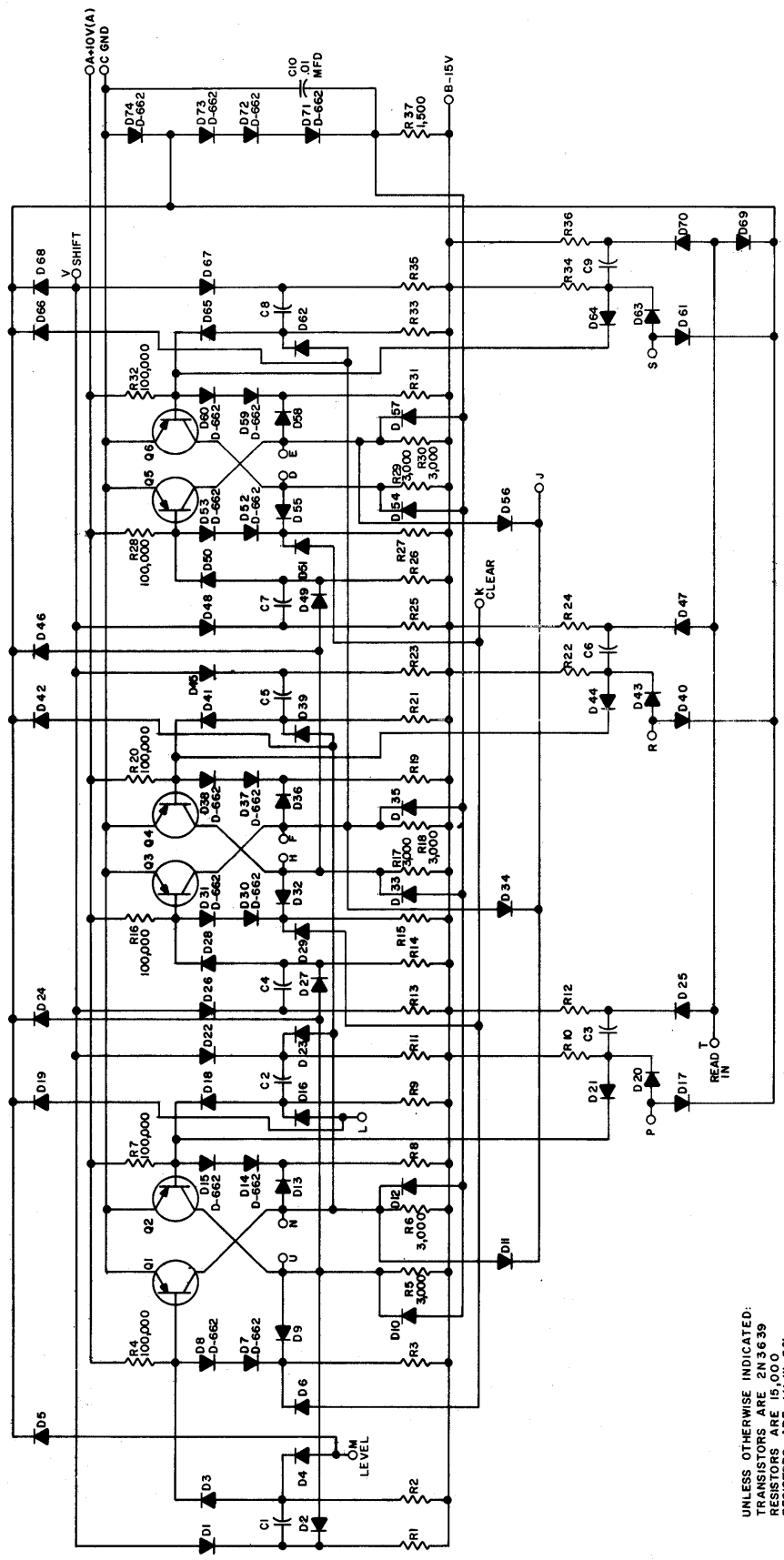


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC3639
CAPACITORS ARE 82 MMFD
RESISTORS ARE 1/8W; 5%
RESISTORS ARE 15,000
DIODES ARE D-664

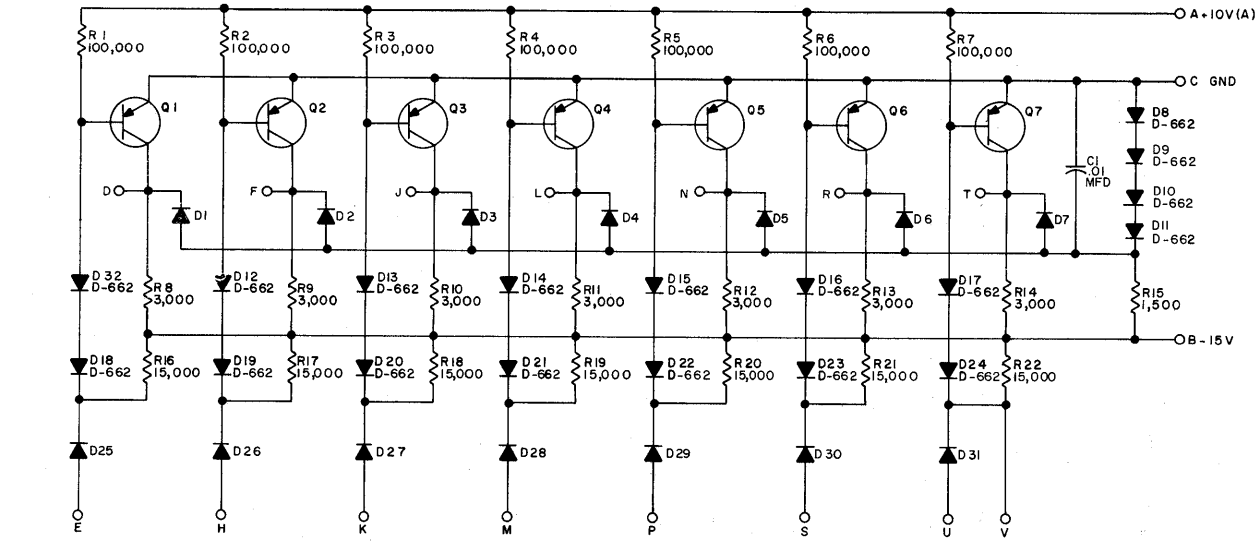
RS-D-R211 MA, MB, PC



UNLESS OTHERWISE INDICATED:
DIODES ARE D-664
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4W, 5%

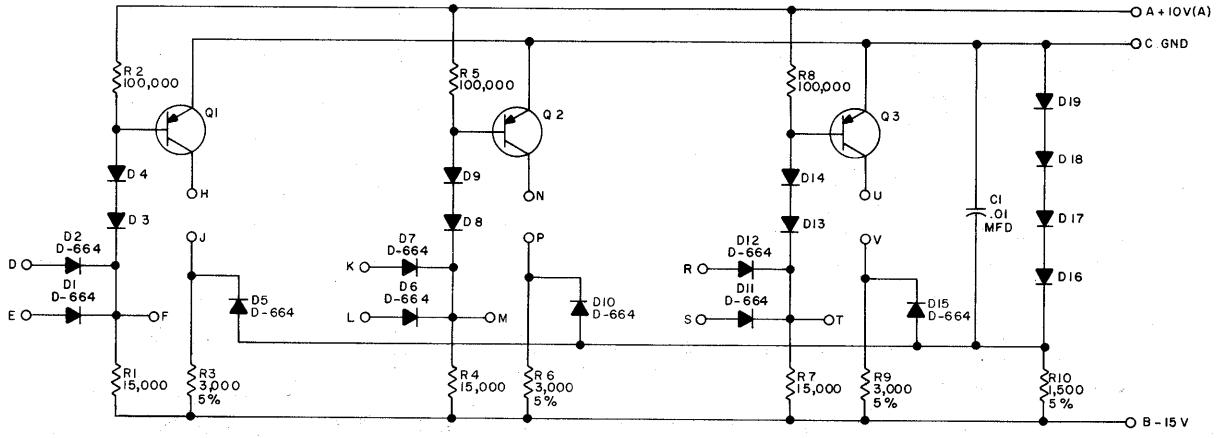


RS-C-R220 3-Bit Shift Register



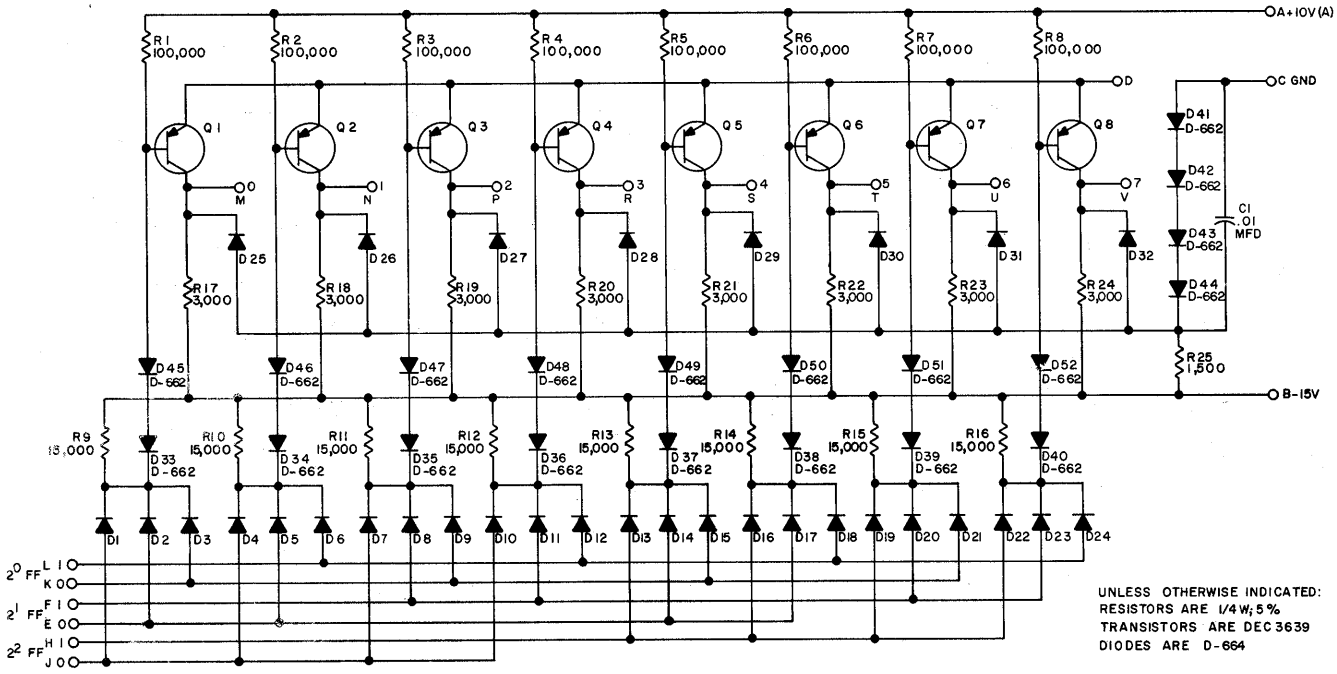
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639

RS-B-S107 Inverter

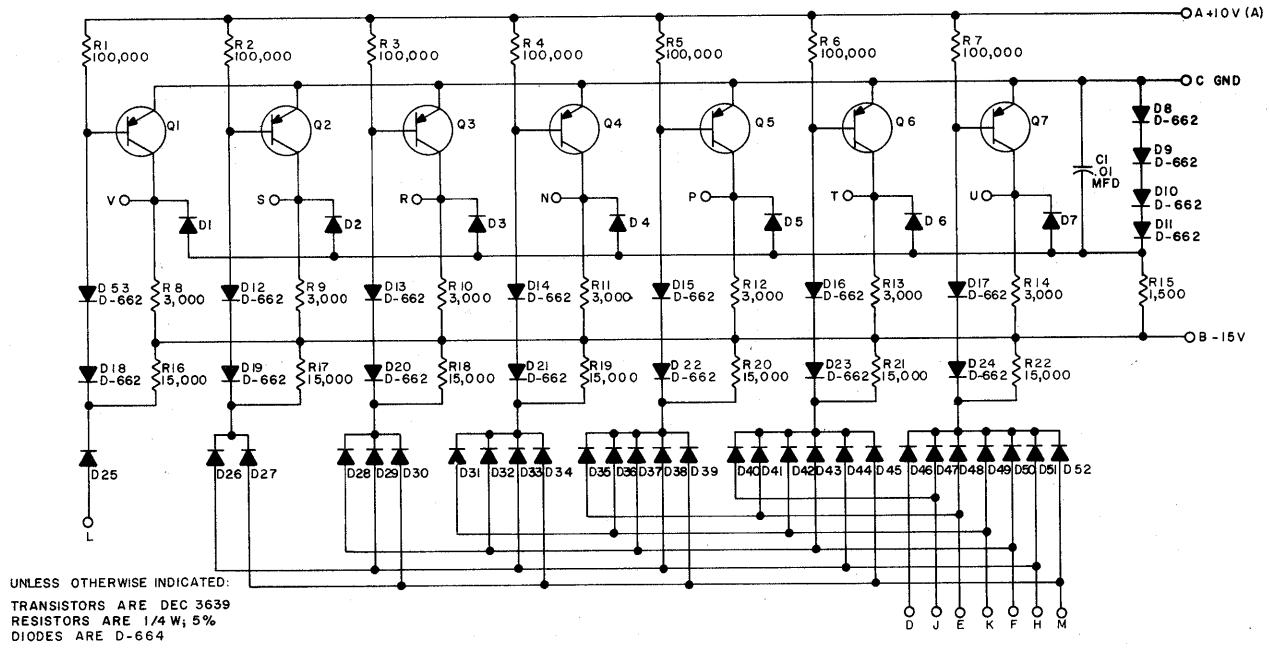


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4W;10%
DIODES ARE D-662

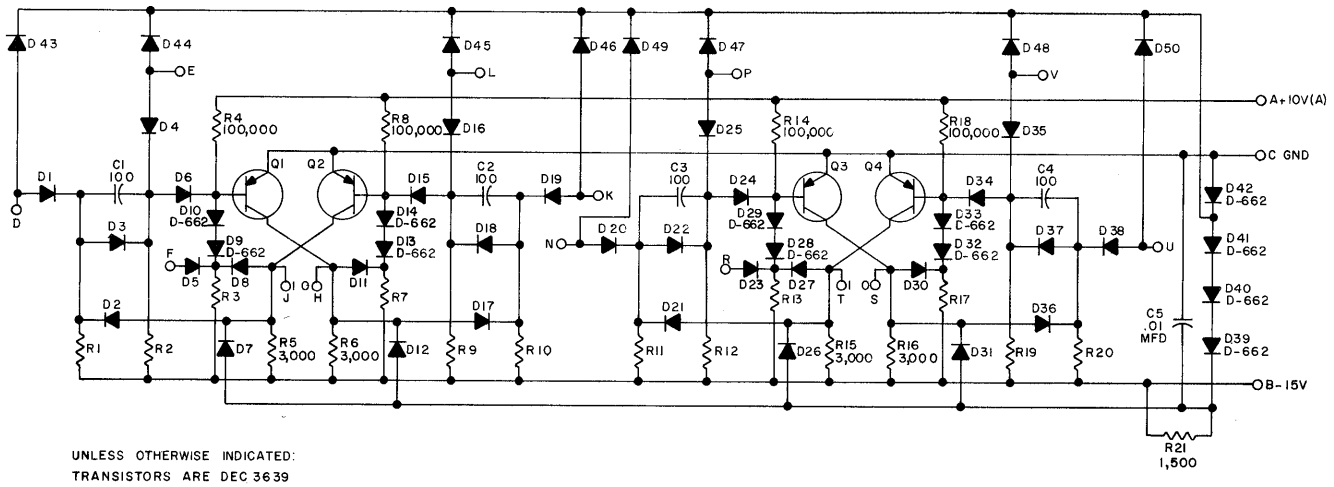
RS-B-S111 Diode Gate



RS-B-S151 Binary-to-Octal Decoder

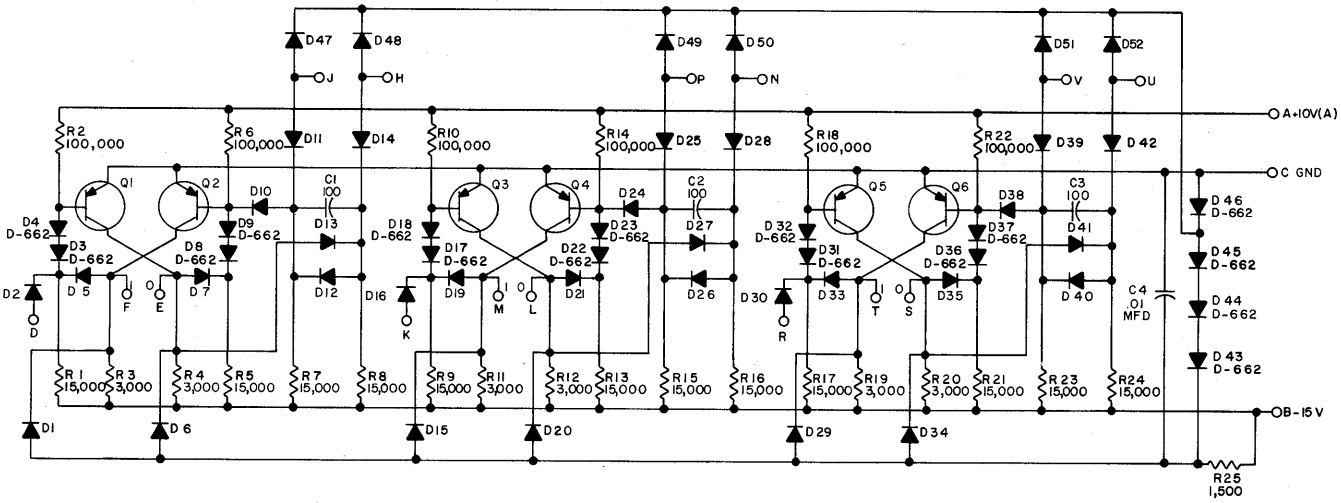


RS-B-S181 DC Carry Chain



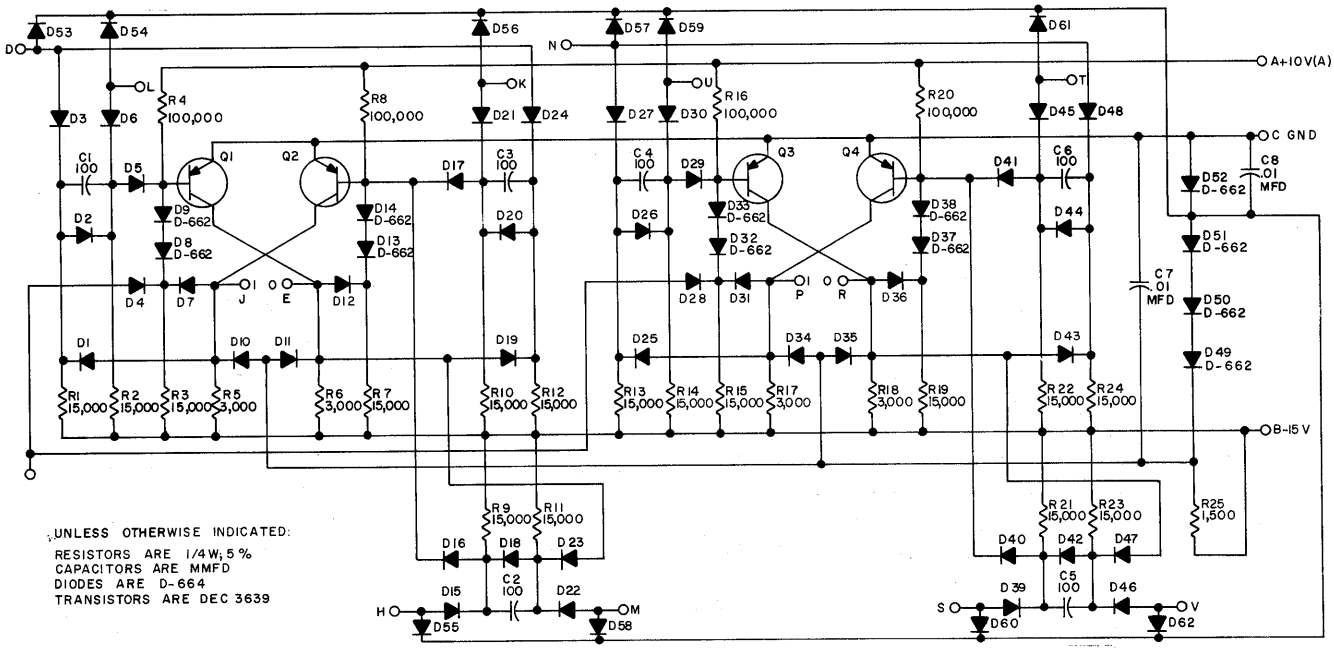
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 15,000
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

RS-B-S202 Dual Flip-Flop

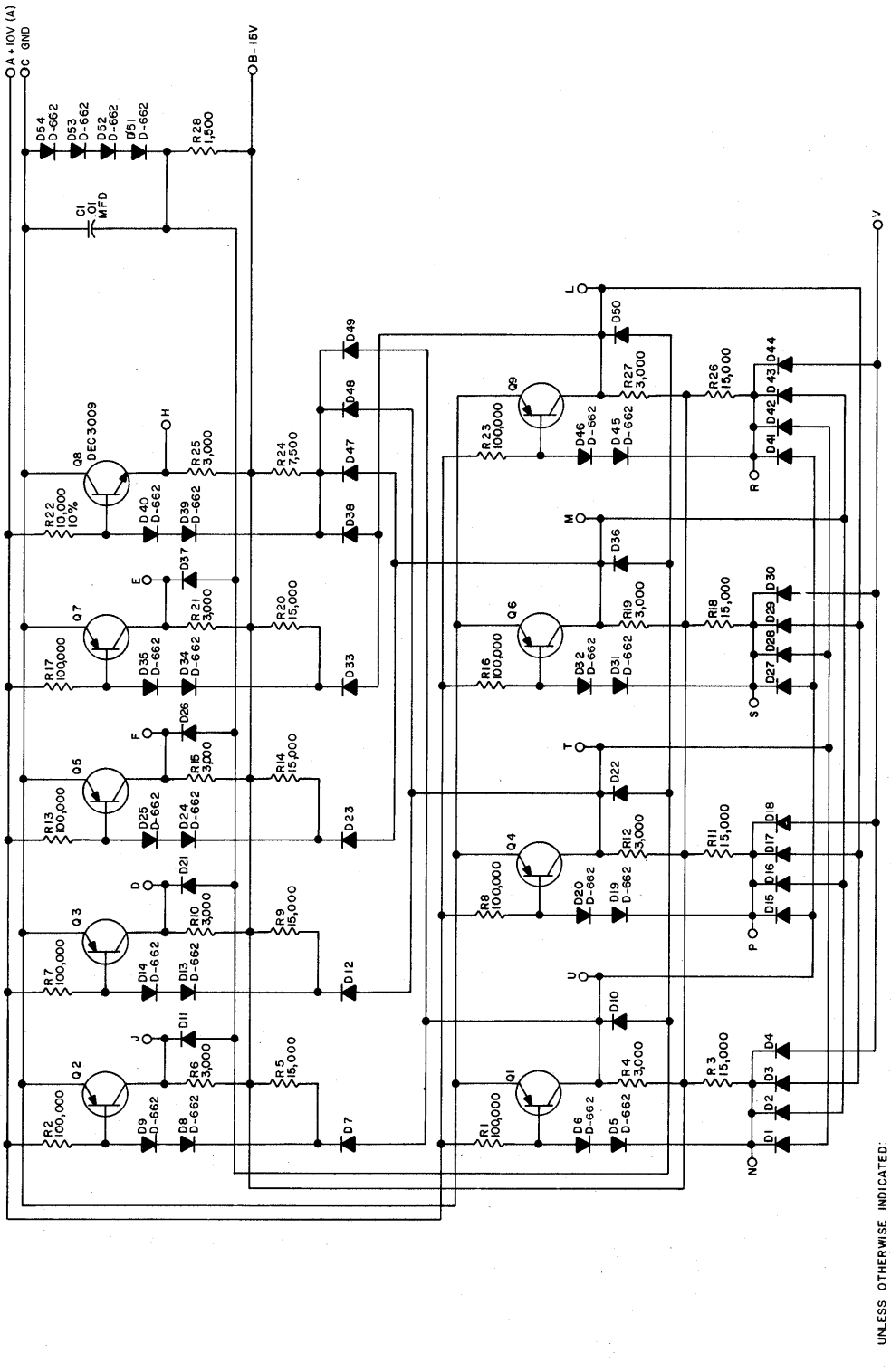


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639

RS-B-S203 Triple Flip-Flop

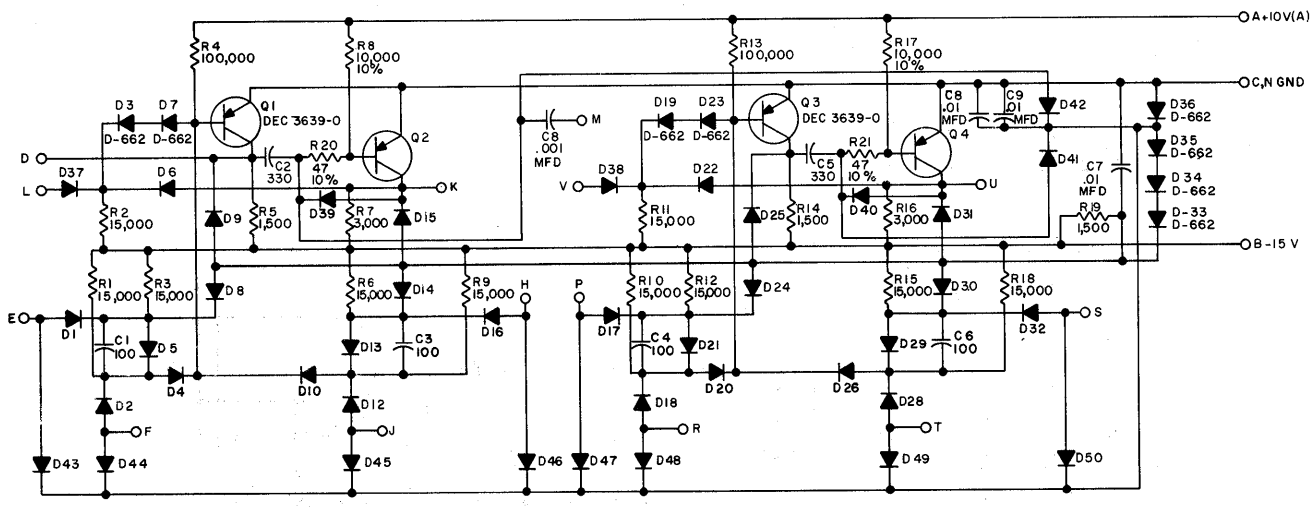


RS-B-S205 Dual Flip-Flop



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
TRANSISTORS ARE DEC 3639
DIODES ARE D-664

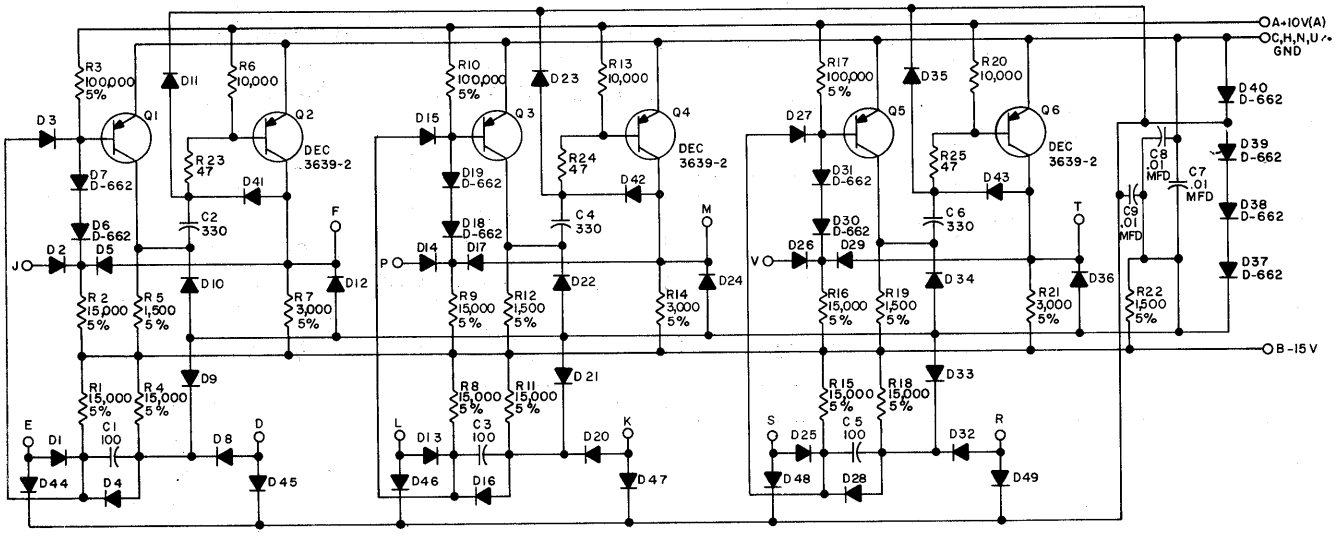
RS-C-S284 Quadraflop



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-2

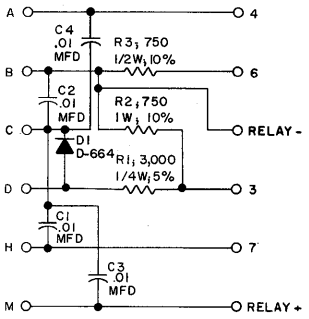
RS-B-S602 Pulse Amplifier



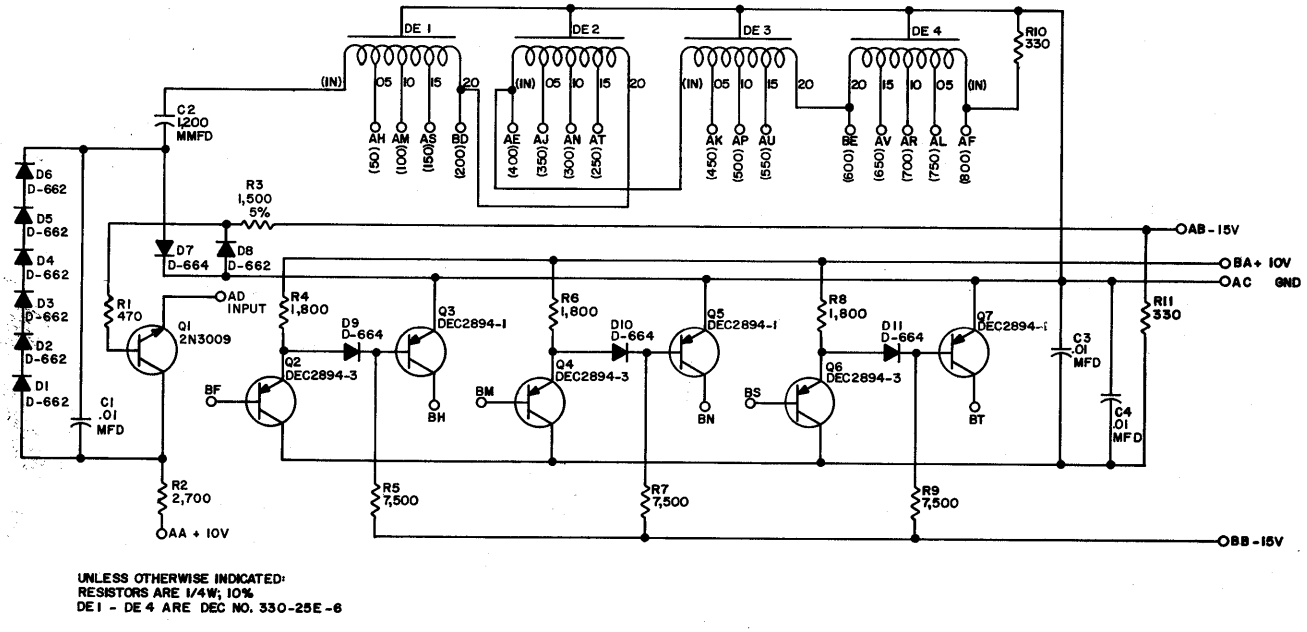
UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-0

RS-B-S603 Pulse Amplifier

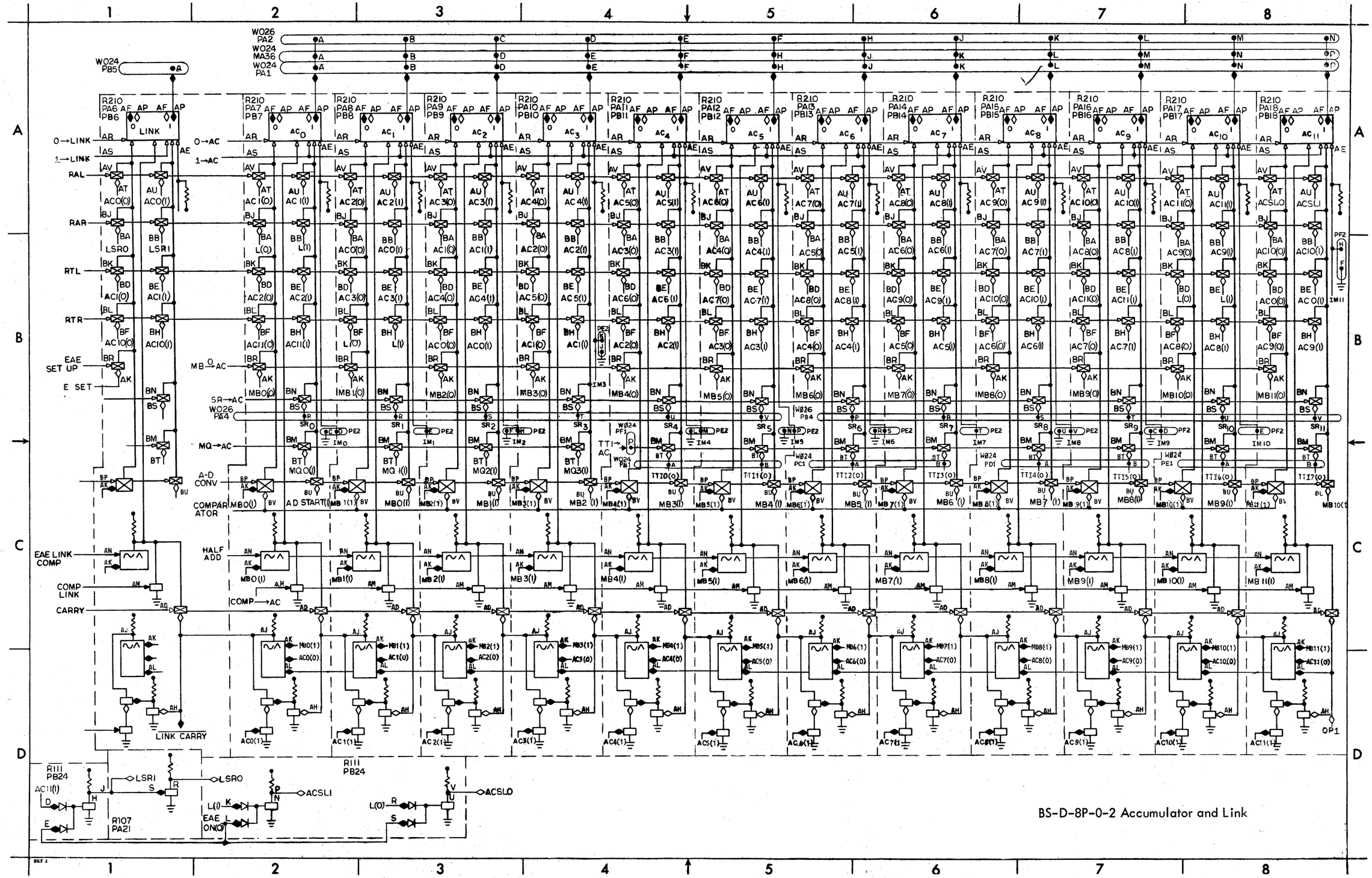


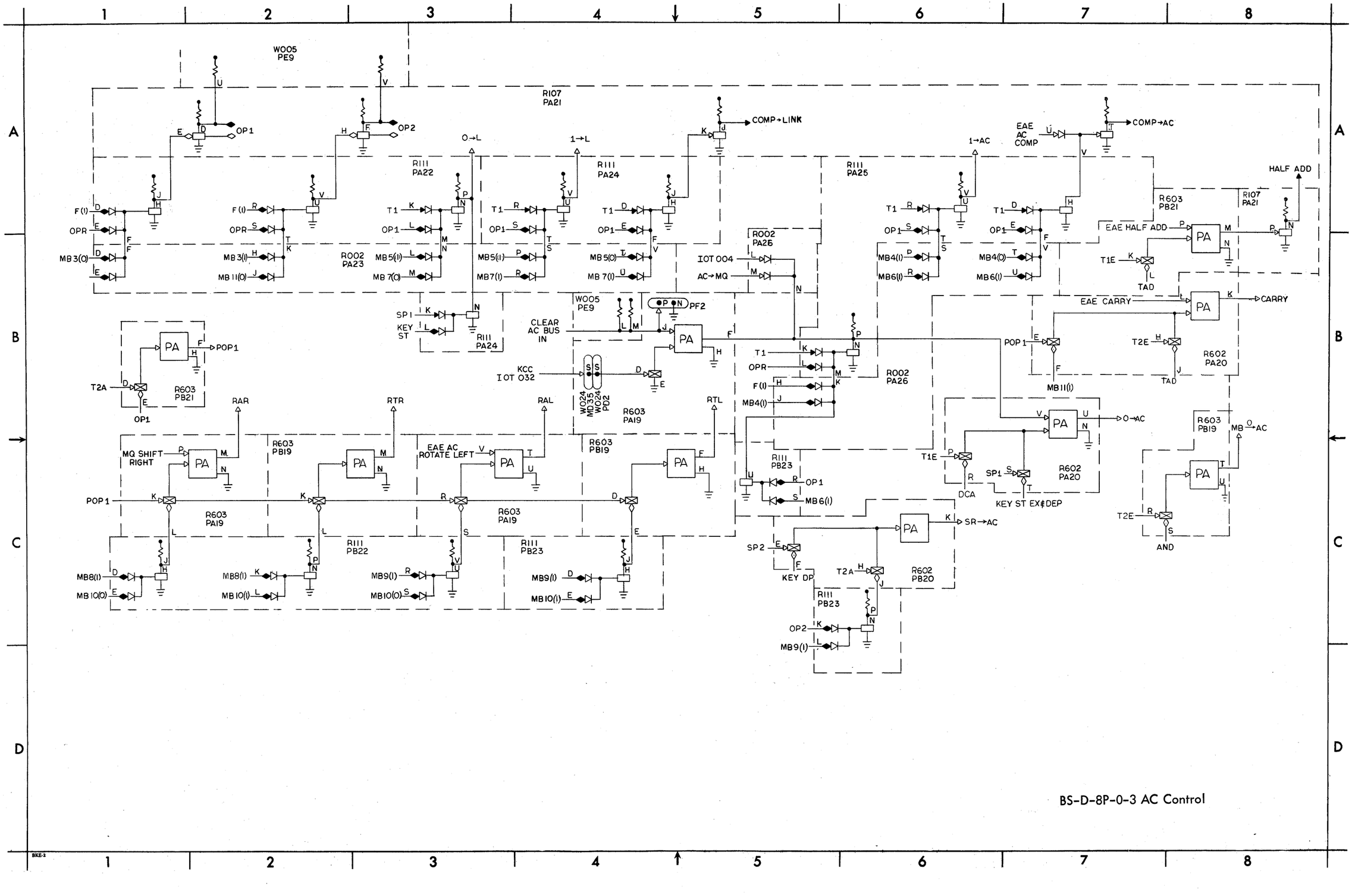
RS-B-W070 Teletype Connector



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DE1 - DE 4 ARE DEC NO. 330-25E-6

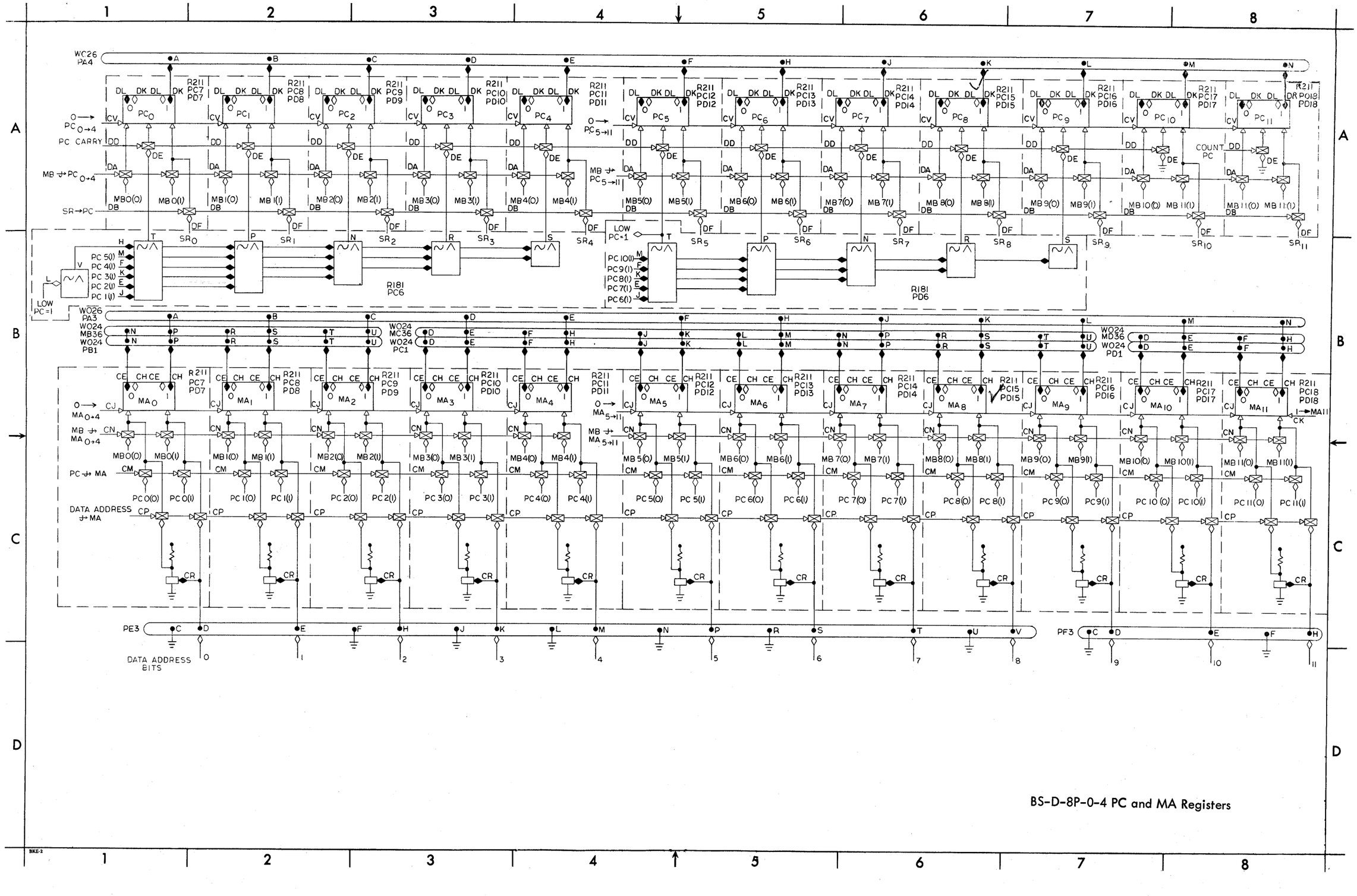
RS-B-W300 Delay Line


1
2
3
4
5
6
7
8
A
B
C
D
W026 PA2
W024 MA36
W024 PA1
W024 PB5
R210 PA6 PB6
LINK
R210 PA7 PB7
AC0
R210 PA8 PB8
AC1
R210 PA9 PB9
AC2
R210 PA10 PB10
AC3
R210 PA11 PB11
AC4
R210 PA12 PB12
AC5
R210 PA13 PB13
AC6
R210 PA14 PB14
AC7
R210 PA15 PB15
AC8
R210 PA16 PB16
AC9
R210 PA17 PB17
AC10
R210 PA18 PB18
AC11
0→LINK
1→LINK
RAL
RAR
RTL
RTR
EAE SET UP
E SET
0→AC
1→AC
MB 0→AC
SR→AC
W026 PB4
MQ→AC
A-D CONV
COMPARATOR
EAE LINK COMP
COMP LINK
CARRY
HALF ADD
COMP→AC
LINK CARRY
R111 PB24
R107 PA21
W024 PF1
W024 PB1
W024 PC1
W024 PD1
W024 PE1
PE2
PF2
IM0
IM1
IM2
IM3
IM4
IM5
IM6
IM7
IM8
IM9
IM10
IM11
OP1
ACSLI
ACSLO
BS-D-8P-0-2 Accumulator and Link

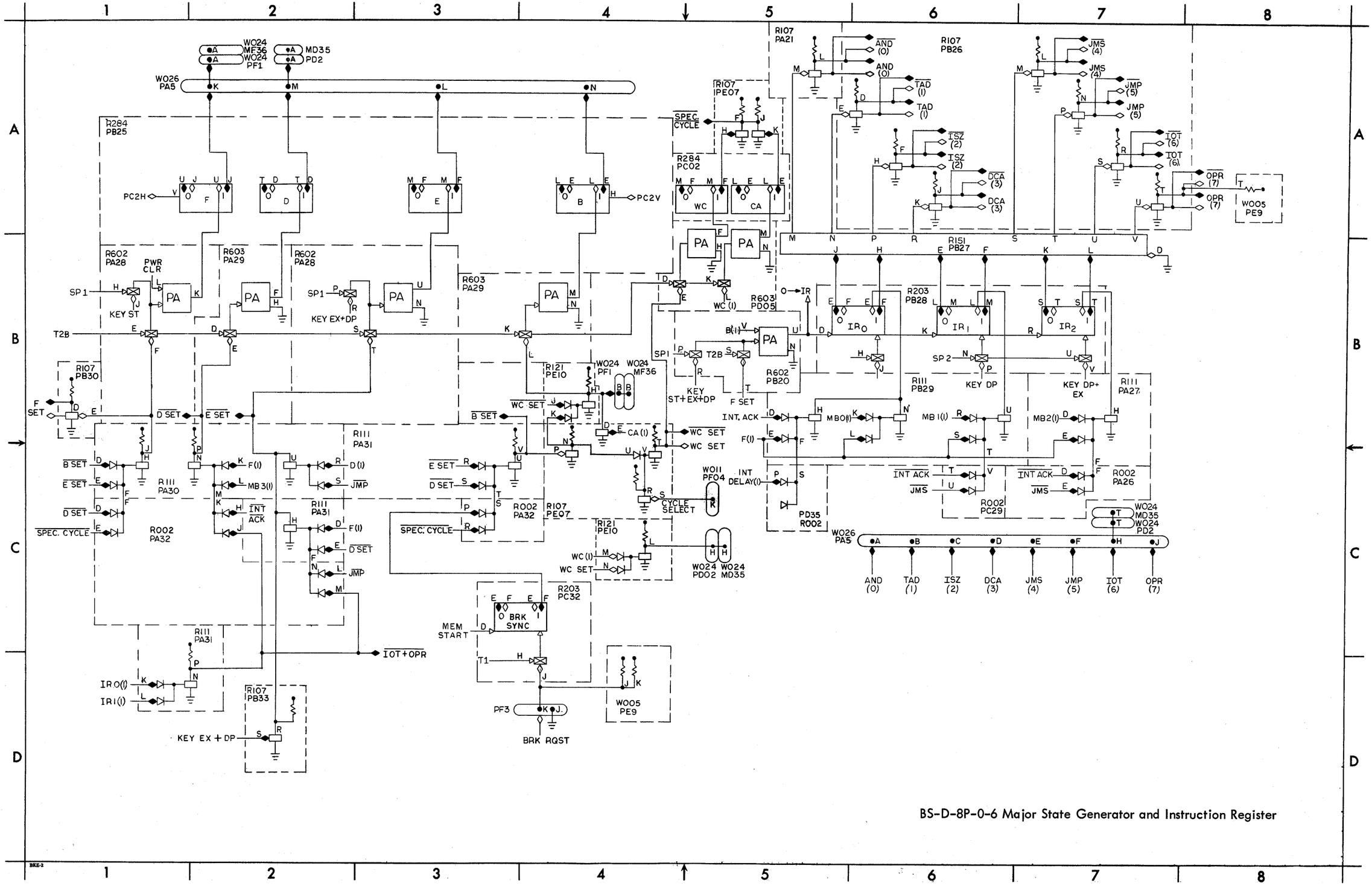


BS-D-8P-0-3 AC Control

BKE-2

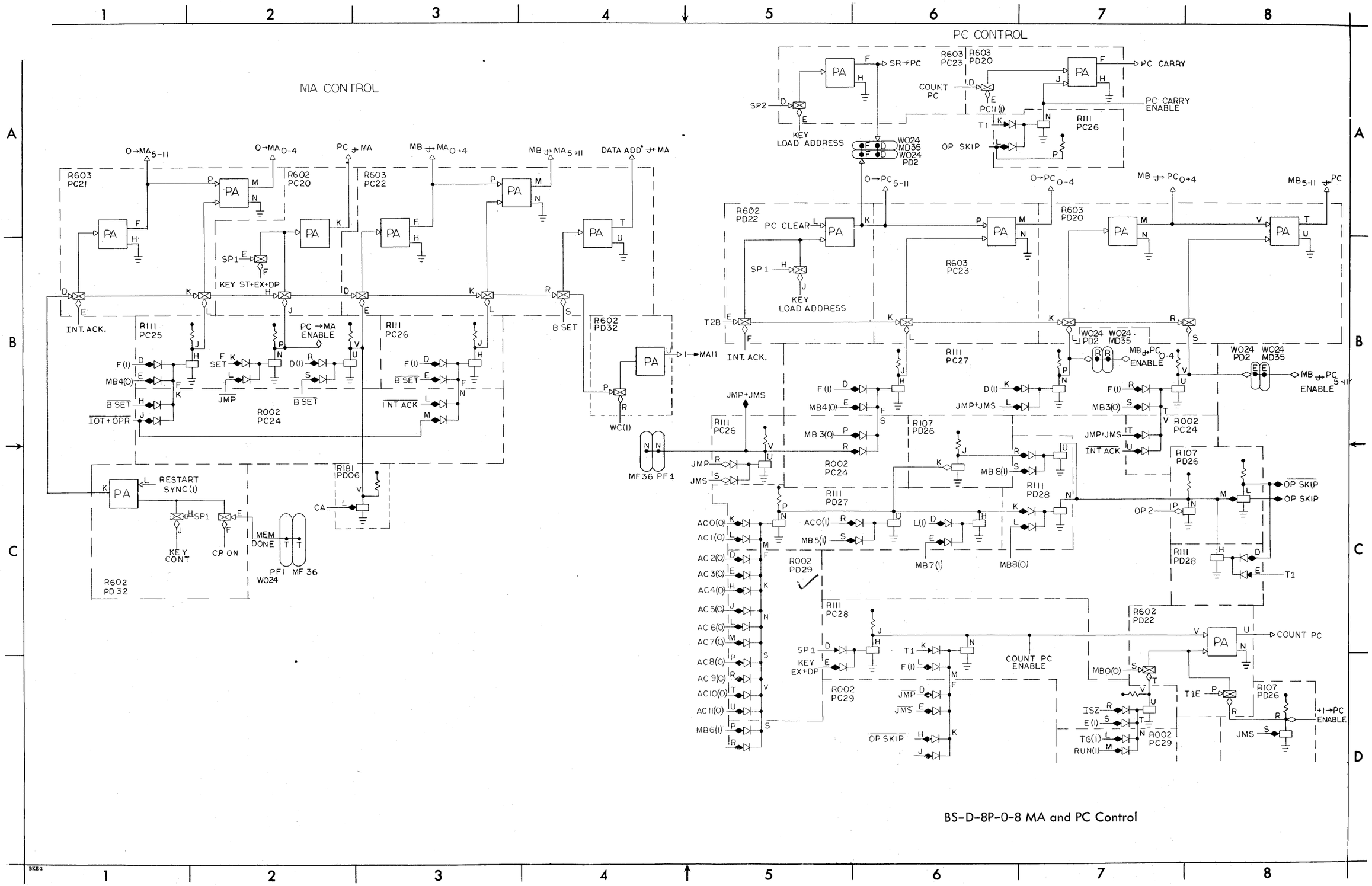


BS-D-8P-0-4 PC and MA Registers



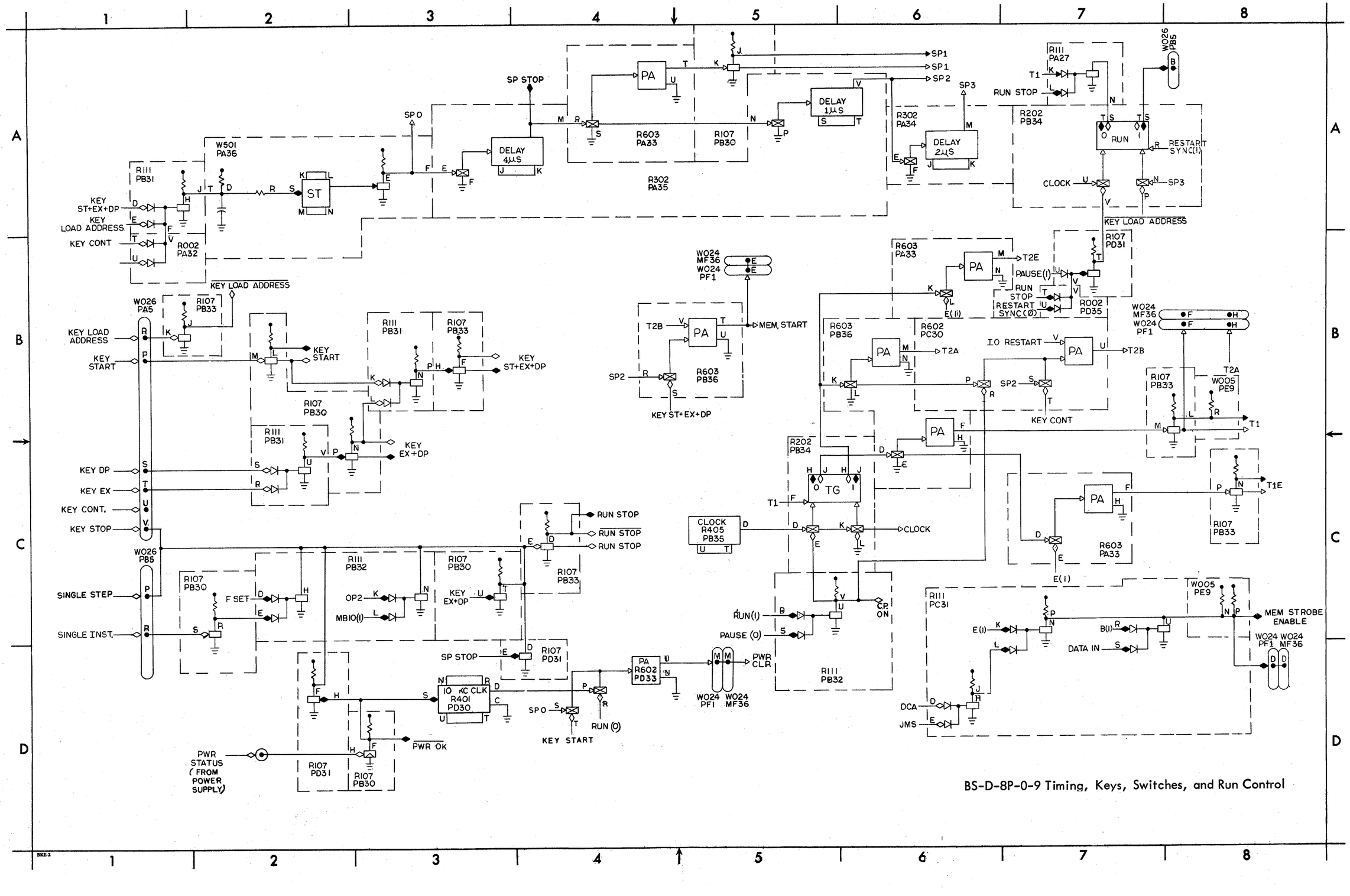
BS-D-8P-0-6 Major State Generator and Instruction Register

BKE-2



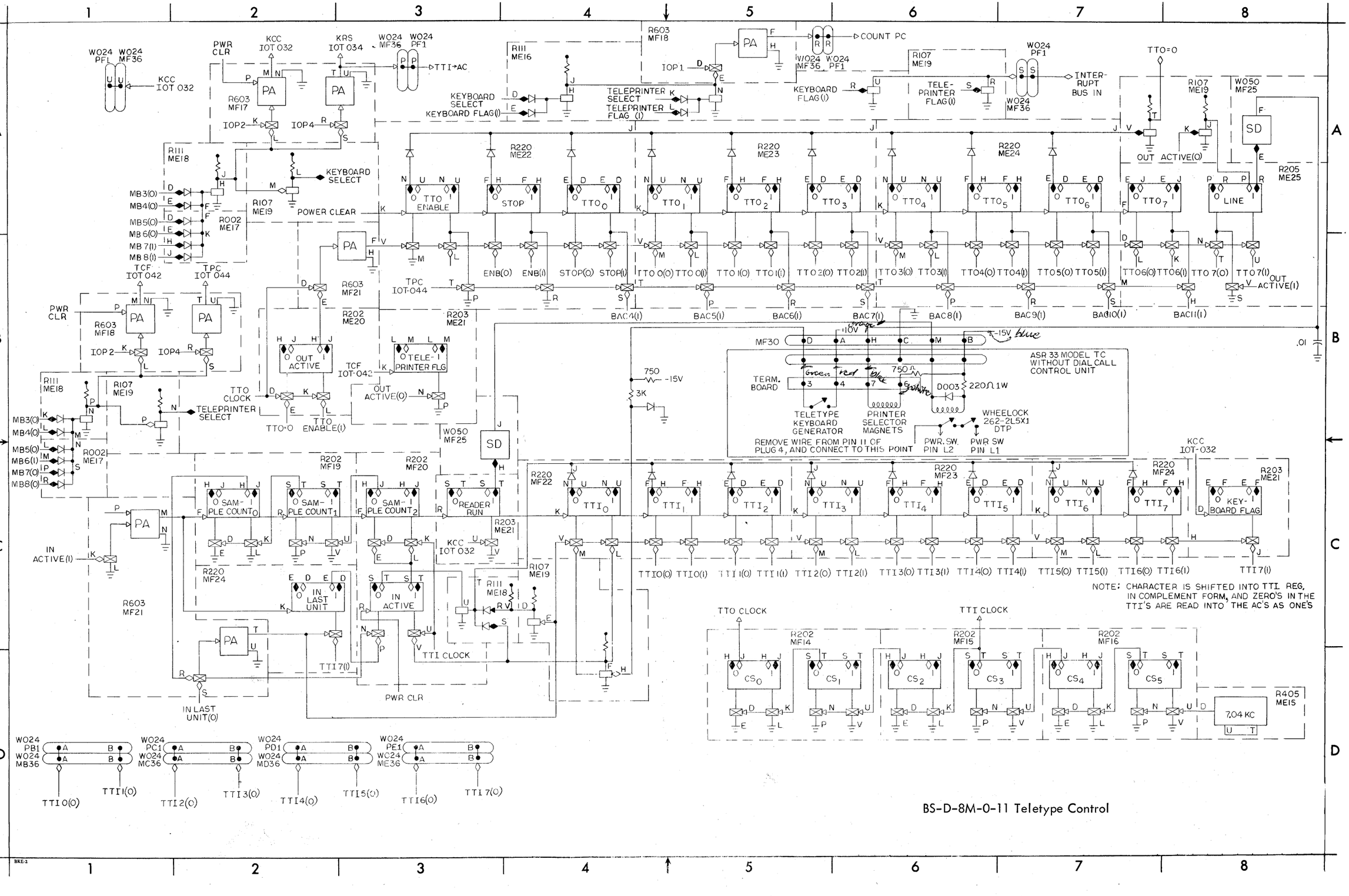
BS-D-8P-0-8 MA and PC Control

BKE-2

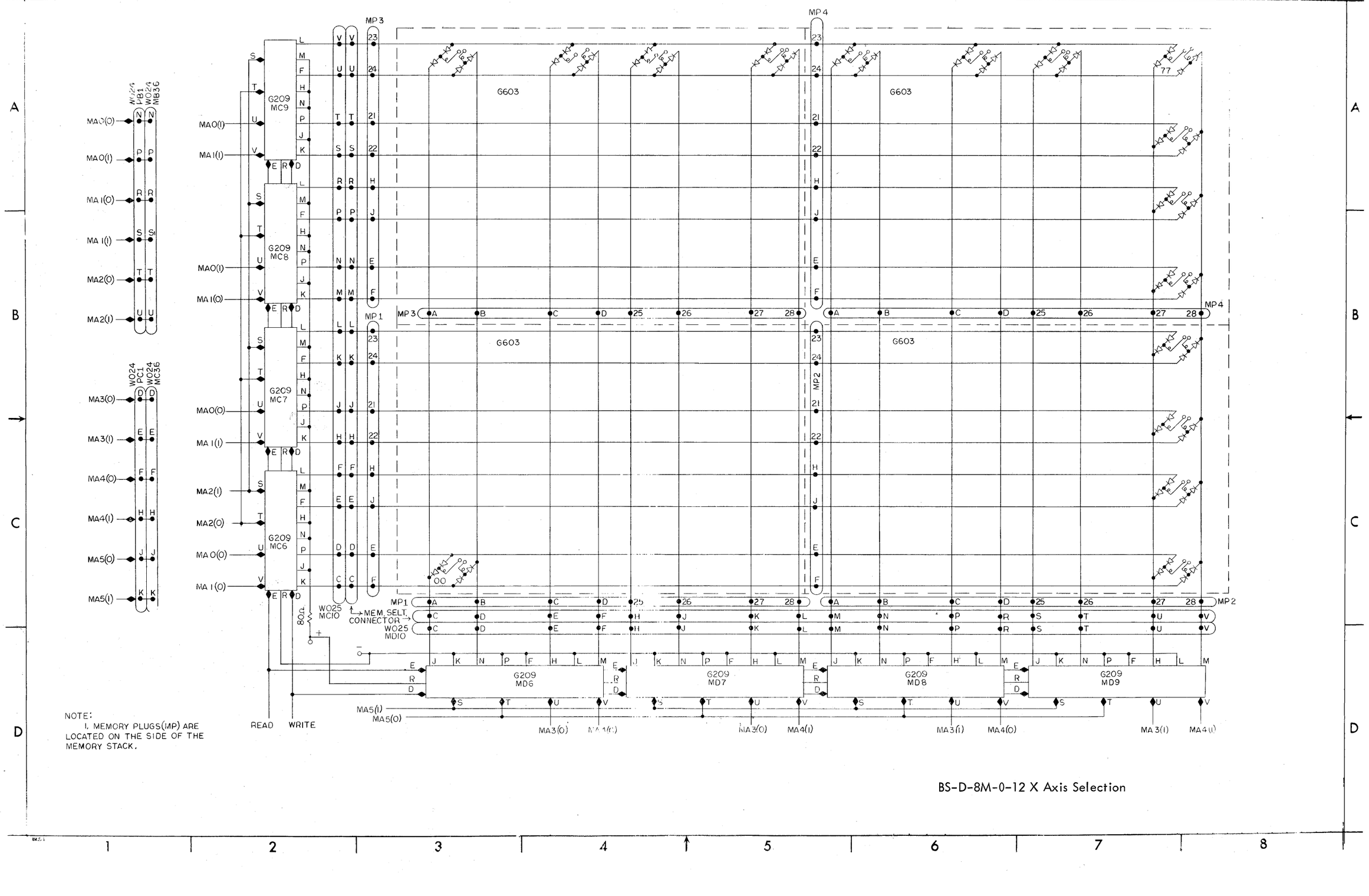


BS-D-8P-0-9 Timing, Keys, Switches, and Run Control

BKE-2


KCC IOT 032
KRS IOT 034
TTI→AC
COUNT PC
INTER-RUPT BUS IN
TTO=0
KEYBOARD SELECT
KEYBOARD FLAG(I)
TELEPRINTER SELECT
TELEPRINTER FLAG (I)
TELE-PRINTER FLAG(I)
POWER CLEAR
TTO ENABLE
STOP
LINE
OUT ACTIVE(O)
OUT ACTIVE(I)
TCF IOT 042
TPC IOT 044
TTO CLOCK
TTO-O
TTO ENABLE(I)
OUT ACTIVE
TELE-PRINTER FLG
TELEPRINTER SELECT
IN ACTIVE(I)
IN LAST UNIT
IN LAST UNIT(O)
READER RUN
TTI CLOCK
PWR CLR
ASR 33 MODEL TC WITHOUT DIAL CALL CONTROL UNIT
TERM. BOARD
TELETYPE KEYBOARD GENERATOR
PRINTER SELECTOR MAGNETS
WHEELOCK 262-2L5X1 DTP
PWR. SW. PIN L2
PWR SW PIN L1
REMOVE WIRE FROM PIN 11 OF PLUG 4, AND CONNECT TO THIS POINT
NOTE: CHARACTER IS SHIFTED INTO TTI REG, IN COMPLEMENT FORM, AND ZERO'S IN THE TTI'S ARE READ INTO THE AC'S AS ONE'S
TTO CLOCK
TTI CLOCK
7.04 KC
BS-D-8M-0-11 Teletype Control

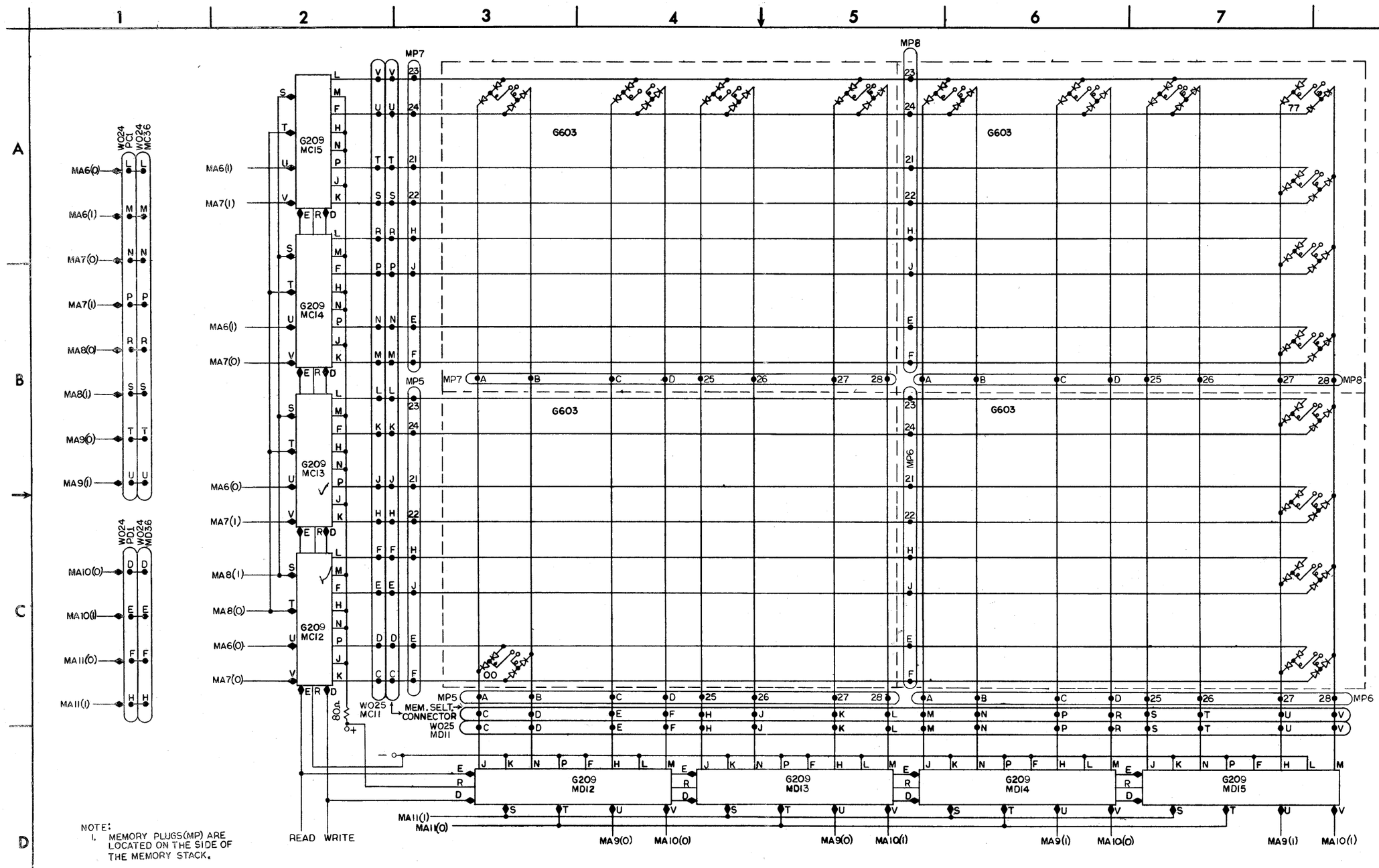
BS-D-8M-0-12 X Axis Selection



NOTE:
1. MEMORY PLUGS(MP) ARE LOCATED ON THE SIDE OF THE MEMORY STACK.

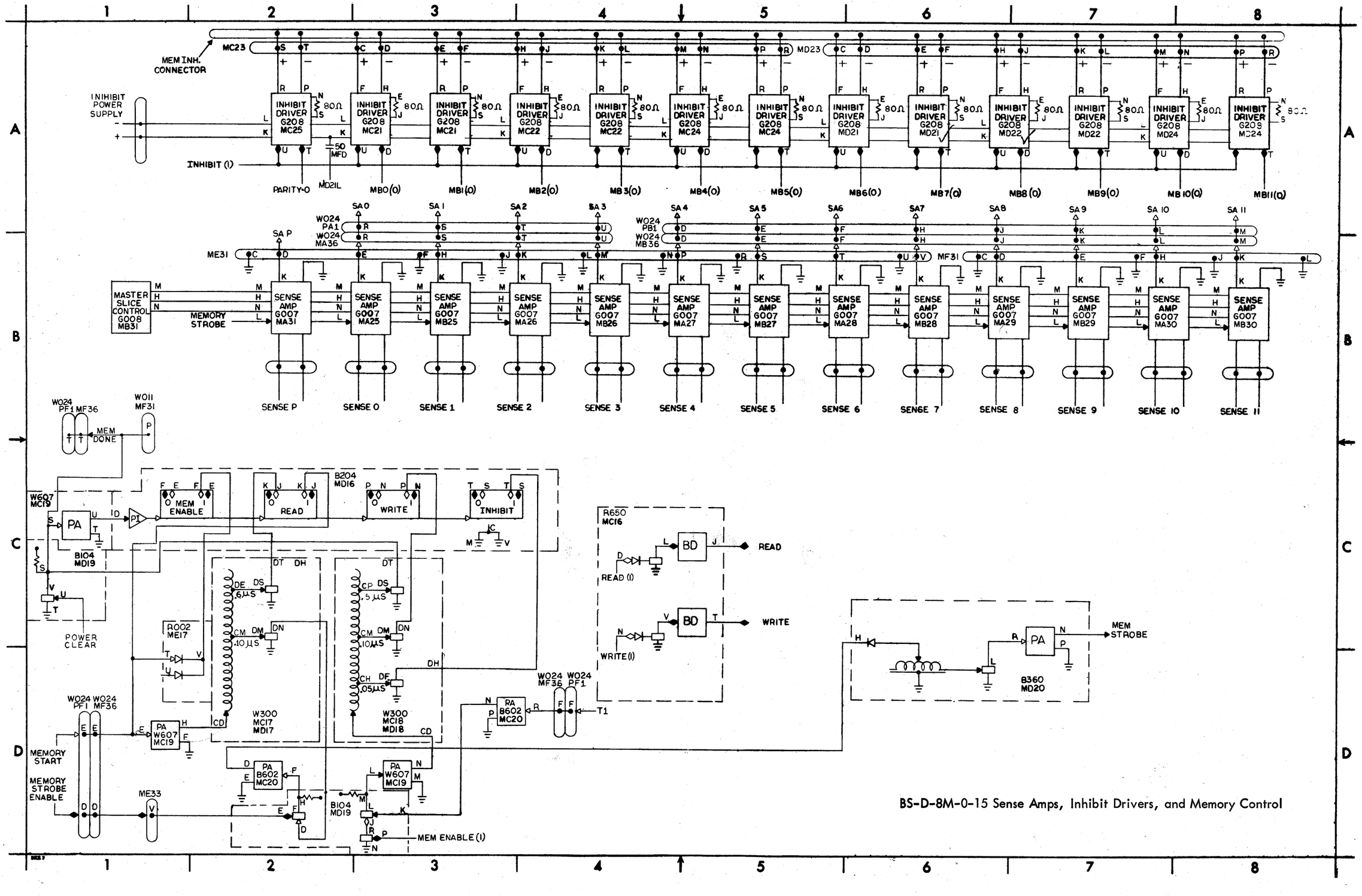
BS-D-8M-0-12 X Axis Selection

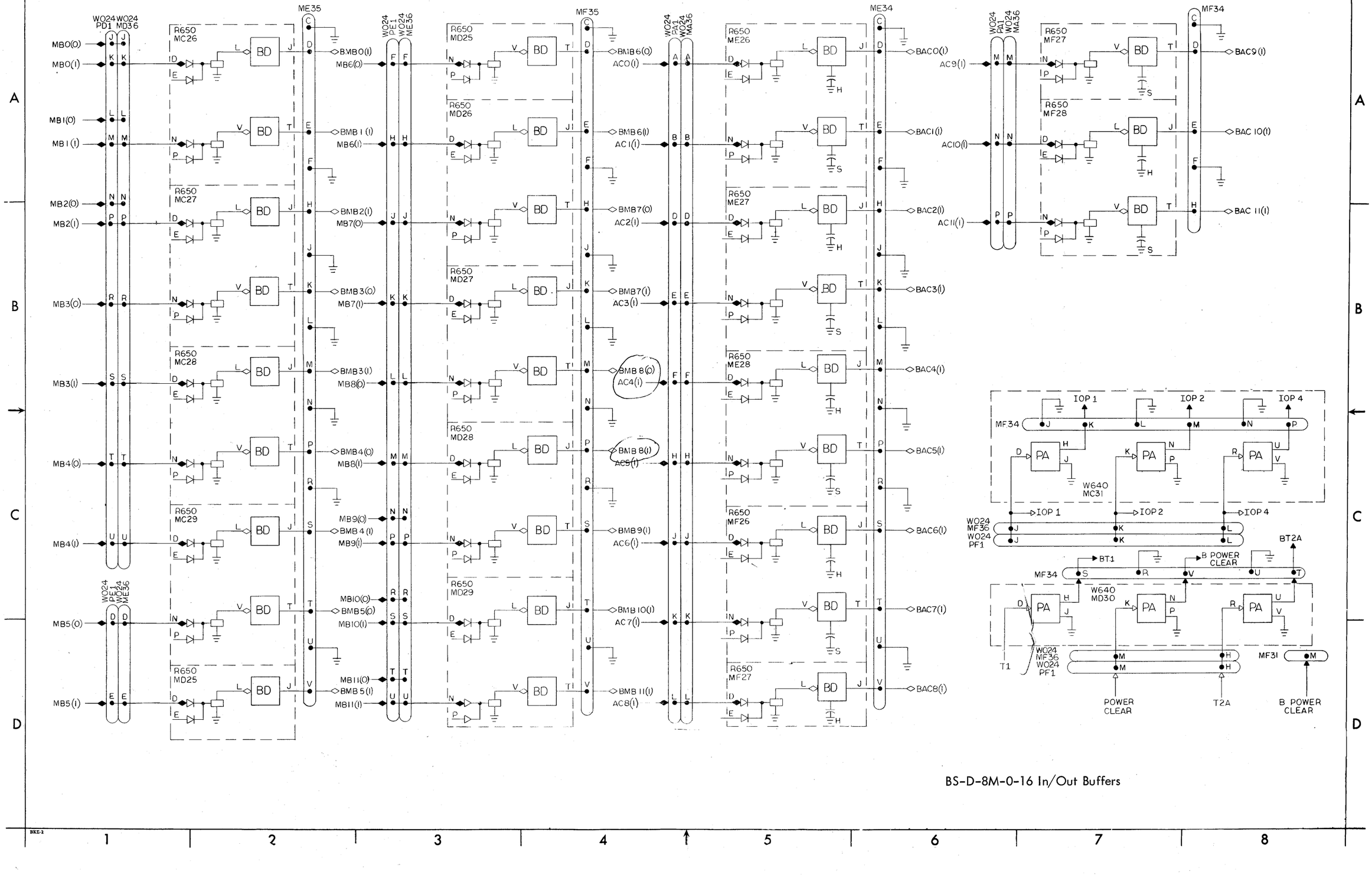
BS-D-8M-0-13 Y Axis Selection



NOTE:
1. MEMORY PLUGS(MP) ARE LOCATED ON THE SIDE OF THE MEMORY STACK.

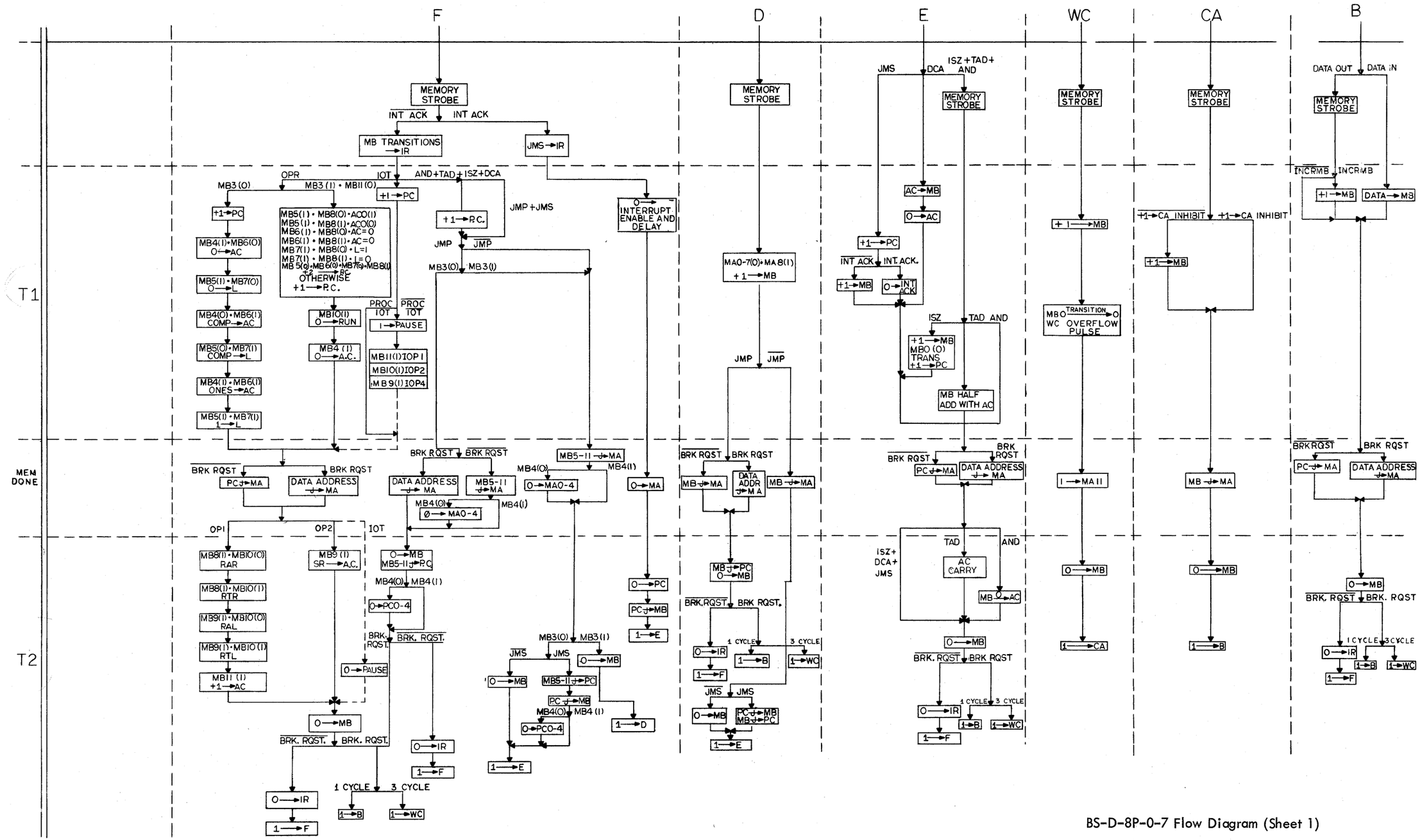
BS-D-8M-0-13 Y Axis Selection


MEM INH. CONNECTOR
MC23
MD23
INHIBIT POWER SUPPLY
INHIBIT DRIVER G208 MC25
INHIBIT DRIVER G208 MC21
INHIBIT DRIVER G208 MC22
INHIBIT DRIVER G208 MC24
INHIBIT DRIVER G208 MD21
INHIBIT DRIVER G208 MD22
INHIBIT DRIVER G208 MD24
INHIBIT DRIVER G208 MD24
80Ω
50 MFD
INHIBIT (1)
PARITY-0
MD21L
MB0(0)
MB1(0)
MB2(0)
MB3(0)
MB4(0)
MB5(0)
MB6(0)
MB7(0)
MB8(0)
MB9(0)
MB10(0)
MB11(0)
SA P
SA 0
SA 1
SA 2
SA 3
SA 4
SA 5
SA 6
SA 7
SA 8
SA 9
SA 10
SA 11
W024 PA1
W024 MA36
W024 PB1
W024 MB36
ME31
MF31
MASTER SLICE CONTROL G008 MB31
MEMORY STROBE
SENSE AMP G007 MA31
SENSE AMP G007 MA25
SENSE AMP G007 MB25
SENSE AMP G007 MA26
SENSE AMP G007 MB26
SENSE AMP G007 MA27
SENSE AMP G007 MB27
SENSE AMP G007 MA28
SENSE AMP G007 MB28
SENSE AMP G007 MA29
SENSE AMP G007 MB29
SENSE AMP G007 MA30
SENSE AMP G007 MB30
SENSE P
SENSE 0
SENSE 1
SENSE 2
SENSE 3
SENSE 4
SENSE 5
SENSE 6
SENSE 7
SENSE 8
SENSE 9
SENSE 10
SENSE 11
W024 PF1 MF36
W011 MF31
MEM DONE
W607 MC19
PA
PI
B104 MD19
MEM ENABLE
READ
WRITE
INHIBIT
B204 MD16
POWER CLEAR
R002 ME17
W300 MC17 MD17
W300 MC18 MD18
DE .6μS
CP .5μS
CM .10μS
CH .05μS
DS
DM
DN
DT
DH
CD
PA W607 MC19
PA B602 MC20
RA B602 MC20
W024 MF36 PF1
T1
R650 MC16
BD
READ (1)
WRITE (1)
MEMORY START
MEMORY STROBE ENABLE
ME33
MEM ENABLE (1)
B360 MD20
MEM STROBE
BS-D-8M-0-15 Sense Amps, Inhibit Drivers, and Memory Control



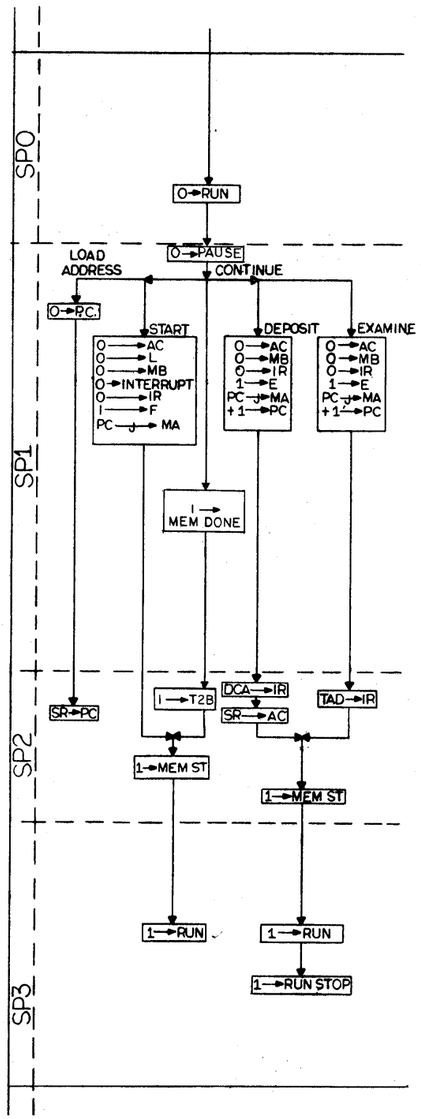
BS-D-8M-0-16 In/Out Buffers

BS-D-8P-0-7 Flow Diagram (Sheet 1)



BS-D-8P-0-7 Flow Diagram (Sheet 1)

BS-D-8P-0-7 Flow Diagram (Sheet 2)



BS-D-8P-0-7 Flow Diagram (Sheet 2)

WD-D-8-0-14 Bus Bar for Power and Logic Wiring

WD-D-8-0-14 Bus Bar for Power and Logic Wiring

	1	2	3	4	5	6	7	8	9	10	11	12
PA	W024: MEMORY CHASSIS CONNECTOR	W026: INDICATOR CONNECTOR AC Ø-11	W026: INDICATOR CONNECTOR MA Ø-11	W026: INDICATOR CONNECTOR PC Ø-11 SR Ø-5	W026: INDICATOR CONNECTOR INSTR. STATES KEYS	R210: [illegible]C	R210: AC 0	R210: AC 1	R210: AC 2	R210: AC 3	R210: AC 4	R210: AC 5
PB	W024: MEMORY CHASSIS CONNECTOR		W026: INDICATOR CONNECTOR MB Ø-11	W026: INDICATOR CONNECTOR MQ Ø-11 SR 6-11	W026: INDICATOR CONNECTOR LINK RUN P2955 ION SING STEP SING INST.	LINC	AC 0	AC 1	AC 2	AC 3	AC 4	AC 5
PC	W024: MEMORY CHASSIS CONNECTOR	R284: S; C; WC; CA	R603✡: 1→S; 1→C; RAR	R121✡: +1→PC; COUNT MB ENABLE; MB=3; C SET	R111✡: SHIFT MB; MB=3; TT INST	R181: HIGH PC CARRY	R[illegible]: MB MA PC 0	R211: MB 1 MA 1 PC 1	R211: MB 2 MA 2 PC 2	R211: MB 3 MA 3 PC 3	R211: MB 4 MA 4 PC 4	R211: MB 5 MA 5 PC 5
PD	W024: MEMORY CHASSIS CONNECTOR	W024: MEMORY CHASSIS CONNECTOR	R113✡: S SET; T1S; SHIFT MB; C SET + S SET; RAR	R002✡: TT INST; TT INST; TT INST	R603: WC SET; CA SET; WC OVERFLOW	R181: LOW PC CARRY	MB 0 MA 0 PC 0	MB 1 MA 1 PC 1	MB 2 MA 2 PC 2	MB 3 MA 3 PC 3	MB 4 MA 4 PC 4	MB 5 MA 5 PC 5
PE	W024: MEMORY CHASSIS CONNECTOR	W011: IN-OUT CONNECTOR IM Ø-8	W011: IN-OUT CONNECTOR DATA ADDRESS Ø-8	W011: IN-OUT CONNECTOR DATA BITS Ø-8	R123✡: MB 0 SHIFT ENABLE	R107✡: MB=3; C SET + S SET; LINE; SPEC. CYCLE; TT INST; PC→MA ENABLE; T1S	R107: B SET; SPEC. CYCLE; SPEC. CYCLE; +1→MB ENABLE; B SET; WC SET; WC SET	R65Ø: B RUN; B BREAK	W005: LOADS D THROUGH R	R121: +1→MB ENABLE; B SET; FORCE BANK 0; WC OVERFLOW	A502 △: COMPARATOR	R203 △: AD ENABLE; AD START; PWR LOW
PF	W024: MEMORY CHASSIS CONNECTOR	W011: IN-OUT CONNECTOR IM 9-11 SKIP INTERRUPT) AC RUN	W011: IN-OUT CONNECTOR DATA ADDRESS 9-11 ADDRESS ACCEPTED BREAK	W011: IN-OUT CONNECTOR DATA BITS 9-11	R107 □: INTERRUPT; PWR OK; RESTART; PWR STATUS; START; IOP 2; SKIP	R002 □: SKIP; SKIP; SKIP; SKIP	R302 □: RESTART; RESTART	W501 □: POWER STATUS	R602 □: PWR RESTART	W640: ADDRESS ACCEPTED; WC OVERFLOW	A604 △: D-A CONV. 2 BITS	A604 △: D-A CONV. 2 BITS

	13	14	15	16	17	18	19	20	21	22	23	24
PA	R210: AC 6	R210: AC 7	R210: AC 8	R210: AC 9	R210: AC 1Ø	R210: AC 11	R603: LL AC SUB; RAR; RAL	R602: CARRY; Ø→AC	R107: OP 1; OP 2; COMP→L; AND; HALF ADD; LSR 0; COMP→AC	R111: OP 1; 0→L; OP 2	R002: OP 1; OP 2; 0→L; 1→L; COMP→L	R111: COMP L; 0→L; 1→L
PB	AC 6	AC 7	AC 8	AC 9	AC 1Ø	AC 11	R602: RTL; [illegible]; MB Ø→AC	R602: SR→AC; Ø→IR	R603: POP 1; HALF ADD; COUNT PC	R111: RAR; RTR; RAL	R111: RTL; SR→AC; 0→AC	R111: LSR 1; ASCL 1; ASCL Ø
PC	R211: MB 6 MA 6 PC 6	R211: MB 7 MA 7 PC 7	R211: MB 8 MA 8 PC 8	R211: MB 9 MA 9 PC 9	R211: MB 1Ø MA 1Ø PC 1Ø	R211: MB 11 MA 11 PC 11	R181: HIGH MB CARRY	R602: PC→J→MA; 0→MB	R603: 0→MA5-11; 0→MAØ-4; COUNT MB	R603: MB→J→MA Ø-4; MB→J→MA 5-11; DATA ADD →J→ MA	R603: SR→PC; 0→PCØ-4; IOT 00	R002: 0→MB; 0→MAØ-4; MB5-11 →J→ MA; 0→PCØ-4; MB5-11→J→PC
PD	MB 5 MA 6 PC 6	MB 7 MA 7 PC 7	MB 8 MA 8 PC 8	MB 9 MA 9 PC 9	MB 1Ø MA 1Ø PC 1Ø	MB 11 MA 11 PC 11	R181: LOW MB CARRY	R603: PC CARRY; MBØ-4 →J→ PC; MB5-11 →J→ PC	R603: DATA MB; AC →J→ MB; PC →J→ MB	R602: 0→PC5-11; COUNT PC	R111: DATA MB; 0→MB; 0→MB	R111: COUNT MB; COUNT MB; COUNT MB
PE	R401 △: AD CLOCK	R302 □△: AD CONV.; PWR OK	R603 ✡△: SHIFT MB; RESTART SYNC.; IOT 004	A704 △: REF. SUPPLY	R111 *: ACSL 0; ACSL 1; IM 4	R123 *: IM 4; IM 5; IM 6; IM 7; IM 8; IM 9	R123 *: IM 8; IM 9; IM 1Ø; IM 11; IM 1Ø; IM 11	R111 *: NORMALIZED; NORMALIZED; [illegible]	R002 *: NORMALIZED; NORMALIZED; NORMALIZED; NORMALIZED; NORMALIZED	R107 *: MQ→AC; SC→AC; SC=Ø; MQ11 SH. LFT. SW.; ATG0 ENB; ATG0 ENB; ATG0 ENB	R603 *: MQ→AC; SC→AC; AC→MQ	R002 *: 0→MQ; SC=Ø; 0→ATG0; 0→ATG1; NORMALIZED
PF	A604 △: D-A CONV. 2 BITS	A601 △: D-A CONV. 3 BITS	A601 △: D-A CONV. 3 BITS	REF. SUPPLY	R212 *: MQ 0; MQ 1	R212 *: MQ 2; MQ 3	R212 *: MQ 4; MQ 5	R212 *: MQ 6; MQ 7	R212 *: MQ 8; MQ 9	R212 *: MQ 1Ø; MQ 11	R602 *: MQ SHIFT RIGHT; MQ SHIFT LEFT	R111 *: 0→MQ; SC=0; MQ SHIFT LEFT SWITCH

	25	26	27	28	29	30	31	32	33	34	35	36
PA	R111: COMP AC; 0→AC; 1→AC	R002: 1→IR 2; 0→AC; 0→AC; 1→AC; COMP→AC	R111: 1→IR 2; 0→RUN; AD PAUSE	R602: 1→F; 1→E	R603: 1→D; 1→B; IO RESTART	R111: 1→F; 1→D; 1→E	R111: 1→D; 1→B; IRO(1) IR1(1)	R002: 1→F; 1→D; 1→E; 1→B; KEY MAN	R603: TIE; T2E; SP1	R302: SP3; IOP1	R302: SP1; SP2	W501: SPØ
PB	R284: MAJOR STATES	R1Ø7: TAD; ISZ; DCA; JMS; JMP; IOT; OP	R151: IR DECODER	R203: IR 0; IR 1; IR 2	R111: 1→IR 0; 1→IR [illegible]; 1→IR 1	R1Ø7: F→SET; POWER OK; SP 1; KEY ST; KEY + EX + DP; SING. INS; RUN STOP	R111: KEY MAN; KEY ST + EX + DP; KEY EX + DP	R111: RUN STOP; RUN STOP; TG ENABLE	R1Ø7: RUN STOP; KEY ST + EXT + DP; KEY LOAD ADD; TI; TIE; E SET; PROCESSOR IOT	R202: T.G. F.F.; RUN F.F.	R4Ø5: CLOCK	R6Ø3: TI; T2A; MEM. START
PC	R111: 0→MAØ-4; PC→MA; MBØ-4 → MA	R111: MB5-11 → MA; PC CARRY; JMP + JMS	R111: 0→PCØ-4; MBØ-4 →J→ PC; MB5-11 →J→ PC	R111: COUNT PC; COUNT PC; COUNT PC	R002: COUNT PC; COUNT PC; COUNT PC; AC=0; 1→IR 1	R602: EAE LINK COMP; T2B	R111: STROBE ENABLE; STROBE ENABLE; STROBE ENABLE	R203: BRK. SYNC F.F.; PAUSE F.F.; RESTART SYNC	R603: IOP1; IOP2; IOP4	R302: IOP2; IOP4	R111: PAUSE; 1→INT ACK; 1→INT DELAY	R203: INT. ACK; INT DELAY; INT ENABLE
PD	R002: COUNT MB; COUNT MB; COUNT MB; COUNT MB	R107: 0→MB; 0→MB; OP→SKIP; OP→SKIP; 1→PC EN; COMPARATOR; COMPARATOR	R111: OP SKIP; OP SKIP; OP SKIP	R111: OP SKIP; OP SKIP; OP SKIP	R002: AC=0; AC=0; AC=0; AC=0; AC=0	R401: PWR CLR	R1Ø7: SP STOP; PWR STOP; MB INCREMENT; MB INCREMENT; INTERRUPT INHIBIT; 0 RUN	R6Ø2: MEM. DONE; 1→MAI	R602: 0 INT DEL + ENABLE; POWER CLEAR	R002: IOT 00; IOT 00; IOT 00; 0→PAUSE; AD PAUSE	R002: SC=0; IO HALT; IO HALT; 1→IRO; 0 RUN	R111: 0→INT ACK; 1→INT ACK; IOT 00
PE	R205 *: ATG0; ATG1	R111 *: ATG1 CLR ENABLE; ATG2 SET ENABLE; ATG2 SET ENABLE	R111 *: MUL. SHIFT ENABLE; RT. SHIFT ENABLE; EAE BEGIN	R002 *: MUL. SHIFT ENABLE; ATG2 SET ENABLE; ATG2 SET ENABLE; EAE STOP ENABLE; LOW SC=1	R6Ø3 *: EAE HALF ADD; EAE CARRY; EAE SETUP	R1Ø7 *: EAE CARRY; EAE ROTATE ENABLE; EAE BEGIN; PC→MA ENABLE; +1→PC ENABLE; EAE INST.; EAE LINK COMP.	R6Ø3 *: EAE CLOCK; EAE AC ROTATE LEFT; EAE SHIFT	R2Ø3 *: EAE ON; EAE RUN	R2Ø3 *: EAE IRØ; EAE IR1; EAE IR2	R111 *: E SET; E SET; EAE BEGIN	R111 *: NORM. RUN. INHIBIT; NORM. RUN INHIBIT; EAE INST.	R111 *: 0→SC; LOW SC=1; DIV OVERFLOW STOP
PF	R2Ø5 *: ATG 2; SC 0	R2Ø5 *: SC 1; SC 2	R2Ø5 *: SC 3; SC 4	R603 *: MB→SC; +1→SC; 1→RESTART SYNC	R111 *: MB→SC; EAE STOP ENABLE; EAE STOP ENABLE	R6Ø2 *: EAE STOP; EAE STOP	R111 *: 1→PAUSE; DIV LAST; MQ SHIFT LEFT ENABLE	R111 *: EAE STOP ENABLE; EAE STOP ENABLE; EAE STOP ENABLE	RØØ2 *: DIV LAST; EAE STOP ENABLE; EAE STOP ENABLE; 1→L; 1→L	R111 *: 0→L; 1→L; LINK COMP	RØØ2 *: 0→L; LINK COMP; EAE BEGIN; EAE INST.; DIV OVERFLOW STOP	R4Ø5 *: EAE CLOCK

* USED ONLY WITH #182 EAE.
△ USED ONLY WITH #189 A-D CONVERTER
□ USED ONLY WITH KR01 POWER INTERRUPT
✡ USED ONLY WITH G81 DATA LINE INTERFACE

UML-E-8P-0-19 Processor Utilization Module List

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
																									G007	G007	G007	G007	G007	G007	G007 △	R603 *	R603 *	R603 *	W026	W024
MA				COMPONENT PLATE CONTAINING INHIBIT DRIVER RESISTORS												MEMORY STACK									SA 0	SA 2	SA 4	SA 6	SA 8	SA 10	SA P	START FIELD 0 START FIELD 1 START FIELD 2	START FIELD 3 START FIELD 4 START FIELD 5	START FIELD 6 START FIELD 7	INDICATOR CONNECTOR DATA FIELD INST FIELD	PROCESSOR CHASSIS CONNECTOR
																									G007	G007	G007	G007	G007	G007	G008	B684 *	B684 *	B684 *	B684 *	W024
MB				COMPONENT PLATE CONTAINING INHIBIT DRIVER RESISTORS												MEMORY STACK									SA 1	SA 3	SA 5	SA 7	SA 9	SA 11	MASTER SLICE CONTROL	BMA0(0) BMA0(1)	BMA1(0) BMA1(1)	BMA2(0) BMA2(1)	BMA3(0) BMA3(1)	PROCESSOR CHASSIS CONNECTOR
	R203 *	R203 *	R151 *	R151 *	R151 *	G209	G209	G209	G209	W025	W025	G209	G209	G209	G209	R650	W300	W300	W607	B602	G208	G208	W025	G208	G208 △	R650	R650	R650	R650		W640 O	B684 *	B684 *	B684 *	B684 *	W024
MC	SF 0 SF 1 SF 2	SF 3 SF 4 SF 5	BRK DECODER	DATA DECODER	INST. DECODER	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	X SELECTION CONNECTOR	Y SELECTION CONNECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	READ WRITE	READ CONTROL DELAY	WRITE CONTROL DELAY	MEMORY START WRITE START CONTROL CLEAR	MEMORY STROBE TI	INHIBIT DRIVER 0 INHIBIT DRIVER 1	INHIBIT DRIVER 2 INHIBIT DRIVER 3	INHIBIT CONNECTOR	INHIBIT DRIVER 4 INHIBIT DRIVER 5	W050 INHIBIT DRIVER PARITY	BMB0(1) BMB1(1)	BMB2(1) BMB3(0)	BMB3(1) BMB4(0)	BMB4(1) BMB5(0)		IOP 1 IOP 2 IOP 4	BMA4(0) BMA4(1)	BMA5(0) BMA5(1)	BMA6(0) BMA6(1)	BMA7(0) BMA7(1)	PROCESSOR CHASSIS CONNECTOR
	R205 *	R205 *	R201 *	R201 *	R201 *	G209	G209	G209	G209	W025	W025	G209	G209	G209	G209	B104			B10H	B360	G208	G208	W025	G208	R650	R650	R650	R650	R650	W640	B684 *	B684 *	B684 *	B684 *	W024 *	W024
MD	IF 0 IF 1	IF 2 INT INHIBIT	DF 0	DF 1	DF 2	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	X SELECTION CONNECTOR	Y SELECTION CONNECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	MEMORY SELECTOR	ENABLE READ WRITE INHIBIT	READ CONTROL DELAY	WRITE CONTROL DELAY	STROBE ENABLE WRITE START MEM ENABLE POWER CLEAR	STROBE DELAY	INHIBIT DRIVER 6 INHIBIT DRIVER 7	INHIBIT DRIVER 8 INHIBIT DRIVER 9	INHIBIT CONNECTOR	INHIBIT DRIVER 10 INHIBIT DRIVER 11	BMB6(1) BMB6(0)	BMB7(1) BMB7(0)	BMB8(1) BMB8(0)	BMB9(1) BMB9(0)	BMB10(1) BMB11(0)	BTI POWER CLEAR BT2A	BMA8(0) BMA8(1)	BMA9(0) BMA9(1)	BMA10(0) BMA10(1)	BMA11(0) BMA11(1)	PROCESSOR CHASSIS CONNECTOR	PROCESSOR CHASSIS CONNECTOR
	R201 *	R201 *	R201 *	R603 *	R603 *	R111 *	R107 *	R107 *	R002 △	R111 △	6130 △	B130 △	B130 △	B130 △	R405	R111	5002	R111	R107	R202	R203	R220	R220	R220	R205	R650	R650	R650		W011 *	W011 *	W011 *	W011 *	W011	W011	W024
ME	IB 0 IB 1	IB 1	IB 2	FIELD → SAVE EXT GO IB → IF	0 → SAVE SAVE → FIELD MB → IB	0 → SAVE IB → IF MEM EXT	BREAK FIELD ENABLE BREAK FIELD ENABLE INST FIELD DISABLE DF 0 BUFFER DF 1 BUFFER DF 2 BUFFER SAVE → FIELD	BRK DECODER BRK DECODER BRK DECODER MEM EXT IB → IF FORCE FIELD 0 JMP + JMS	COUNT PC COUNT PC COUNT PC CLEAR PARITY ERROR CLEAR PARITY ERROR	COUNT PC CLEAR PARITY ERROR INT INHIBIT	PARITY DECODER	PARITY DECODER	PARITY DECODER	PARITY DECODER	CLOCK	KEYBOARD SKIP ENABLE TELEPRINT SKIP ENABLE INTERRUPT	IOT 03 IOT 03 IOT 4 IOT 04 MEM ENABLE	IOT 03 IOT 04 0 → INACTIVE	0 → INACTIVE LINE INVERTER 1 → LINE KEYBOARD SELECT TELEPRINT SELECT INTERRUPT TTO 0	OUT-ACTIVE	KEYBOARD FLAG TELE-PRINTER FLAG READER RUN	ENABLE STOP TTO 0	TTO 1 TTO 2 TTO 3	TTO 4 TTO 5 TTO 6	TTO 7 LINE	BAC0(1) BAC1(1)	BAC2(1) BAC3(1)	BAC4(1) BAC5(1)		IN-OUT CONNECTOR ADDRESS EXTEND 1,2,3 & DE 0-2	MEM. EXT. CONNECTOR SA 0-7 & SA-P	MEM. EXT. CONNECTOR BMA 0-4	MEM. EXT. CONNECTOR START FIELD 1-7 & BT 1 & STROBE ENB	IN-OUT CONNECTOR BAC 0-8	IN-OUT CONNECTOR BMB 0-5	PROCESSOR CHASSIS CONNECTOR
	R111 *	R002 *	R111 *	R002 *	W640 *	R123 *	R123 *	B360 △	B104 \	R603 \	R202 \	B130 \	B130 \	R202 △	R202 ○	R202 ○	R603	R603	R202	R202	R603	R220	R220	R220	W050	R650	R650	R650		W011 *	W011 *	W011 *	W011 *	W011	W011	W024
MF	DATA ENABLE INST ENABLE DF → AC	IF → AC IF → AC SF → AC SF → AC DATA ENABLE	DF → AC IF → AC SF → AC	MEM EXT MEM EXT SAVE → FIELD DF → AC DF → AC	DF → AC IF → AC SF → AC	SF → AC SF → AC SF → AC	IF → AC IF → AC	PARITY STROBE DELAY	MEM STROBE SET PARITY ERROR	COUNT PC CLEAR PARITY ERROR SET PARITY ERROR	PARITY PARITY ERROR	PARITY DECODER	PARITY DECODER	CS 0 CS 1	CS 2 CS 3	CS 4 CS 5	MB J → DF IOT 032 IOT 034	SKIP IOT 42 IOT 044	SAMPL COUNT 0 SAMPLE COUNT 1	SAMPLE COUNT 2 IN-ACTIVE	SHIFT TTO 0 → TTI SHIFT TTI	TTI 0 TTI 1 TTI 2	TTI 3 TTI 4 TTI 5	TTI 6 TTI 7 IN LAST UNIT	LINE SEL. DRIVE READER RUN SEL. DRIVE	BAC6(1) BAC7(1)	BAC8(1) BAC9(1)	BAC10(1) BAC11(1)		TELETYPE CONNECTOR	MEM. EXT. CONNECTOR SA 8-11 & PWR CLR	MEM. EXT. CONNECTOR BMA 4-8	MEM. EXT. CONNECTOR BMA 9-11	IN-OUT CONNECTOR BAC 9-11 IOP 1,2,4 BT 1 BT 2 PWR CLR	IN-OUT CONNECTOR BMB 6-11	PROCESSOR CHASSIS CONNECTOR

* USED ONLY WITH 183 MEMORY EXTENSION CONTROL

△ USED ONLY WITH 188 MEMORY PARITY OPTION

JACK [ ] PLUG [X] FEMALE [ ] MALE [X]	LOCATION, LENGTH, ROUTE PB 03

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PB 03	A	MB 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)	PB 03	N	MB 11 (1)	
W/RED (R)		P		
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-25 Indicator Connectors for MB Bits

JACK ☐ PLUG ☒ FEMALE ☐ MALE ☒	LOCATION, LENGTH, ROUTE PA 02

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PA 02	A	AC 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)	PA 02	N	AC 11 (1)	
W/RED (R)		P		
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-26 Indicator Connectors for AC Bits

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	PA03

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PA 03	A	MA 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)	PA 03	N	MA11 (1)	
W/RED (R)		P		
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-27 Indicator Connectors for MA Bits

JACK [ ] PLUG [X] FEMALE [ ] MALE [X]	LOCATION, LENGTH, ROUTE PA 04

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PA 04	A	PC 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)		N	PC 11 (1)	
W/RED (R)		P	SR 0	
W/ORN (O)		R	1	
W/YEL (Y)		S	2	
W/GRN (N)		T	3	
W/BLU (B)		U	4	
W/VIO (V)	PA 04	V	SR 5	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-28 Indicator Connectors for PC and SR Bits

JACK [ ] PLUG [X] FEMALE [ ] MALE [X]	LOCATION, LENGTH, ROUTE PA 05

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PA 05	A	AND (0)	
W/BRN (Z)		B	TAD (1)	
W/RED (R)		C	ISZ (2)	
W/ORN (O)		D	DCA (3)	
W/YEL (Y)		E	JMS (4)	
W/GRN (N)		F	JMP (5)	
W/BLU (B)		H	IOT (6)	
W/VIO (V)		J	OPR (7)	
W/GRY (G)		K	FETCH (F)	
WHT (W)		L	EXECUTE (E)	
W/BLK (X)		M	DEFER (D)	
W/BRN (Z)		N	BREAK (B)	
W/RED (R)		P	KEY START	
W/ORN (O)		R	KEY LOAD ADDRESS	
W/YEL (Y)		S	KEY DP	
W/GRN (N)		T	KEY EX	
W/BLU (B)		U	KEY CONT	
W/VIO (V)	PA 05	V	KEY STOP	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-29 Indicator Connectors for PA05

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	PAØ1 & MA36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PAØ1A	MA36A	AC0(1)	
W/BRN (Z)	PAØ1B	MA36B	AC1(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	AC2(1)	
W/YEL (Y)	E	E	3(1)	
W/GRN (N)	F	F	4(1)	
W/BLU (B)	H	H	5(1)	
W/VIO (V)	J	J	6(1)	
W/GRY (G)	K	K	7(1)	
WHT (W)	L	L	8(1)	
W/BLK (X)	M	M	9(1)	
W/BRN (Z)	N	N	10(1)	
W/RED (R)	P	P	AC11(1)	
W/ORN (O)	R	R	SA 0	
W/YEL (Y)	S	S	1	
W/GRN (N)	T	T	2	
W/BLU (B)	U	U	SA 3	
W/VIO (V)	PAØ1V	MA36V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 1)

JACK ☐ PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE [X]	PBØ1 & MB36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PBØ1A	MB36A	TTI 0(1)	
W/BRN (Z)	B	B	TTI 1(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	SA 4	
W/YEL (Y)	E	E	5	
W/GRN (N)	F	F	6	
W/BLU (B)	H	H	7	
W/VIO (V)	J	J	8	
W/GRY (G)	K	K	9	
WHT (W)	L	L	10	
W/BLK (X)	M	M	SA 11	
W/BRN (Z)	N	N	MA 0(0)	
W/RED (R)	P	P	MA 0(1)	
W/ORN (O)	R	R	MA 1(0)	
W/YEL (Y)	S	S	MA 1(1)	
W/GRN (N)	T	T	MA 2(0)	
W/BLU (B)	U	U	MA 2(1)	
W/VIO (V)	PBØ1V	MB36V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 2)

JACK ☐ PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE [X]	PCØ1 & MC36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PCØ1A	MC36A	TTI2(1)	
W/BRN (Z)	B	B	TTI3(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	MA 3(0)	
W/YEL (Y)	E	E	3(1)	
W/GRN (N)	F	F	4(0)	
W/BLU (B)	H	H	4(1)	
W/VIO (V)	J	J	5(0)	
W/GRY (G)	K	K	5(1)	
WHT (W)	L	L	6(0)	
W/BLK (X)	M	M	6(1)	
W/BRN (Z)	N	N	7(0)	
W/RED (R)	P	P	7(1)	
W/ORN (O)	R	R	8(0)	
W/YEL (Y)	S	S	8(1)	
W/GRN (N)	T	T	9(0)	
W/BLU (B)	U	U	MA 9(1)	
W/VIO (V)	PCØ1V	MC36V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 3)

JACK ☐ PLUG [X] FEMALE ☐ MALE [X]	LOCATION, LENGTH, ROUTE PDØ1 & MD36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PDØ1A	MD36A	TTI 4(1)	
W/BRN (Z)	B	B	TTI 5(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	MA 10(0)	
W/YEL (Y)	E	E	10(1)	
W/GRN (N)	F	F	11(0)	
W/BLU (B)	H	H	MA 11(1)	
W/VIO (V)	J	J	MB 0(0)	
W/GRY (G)	K	K	0(1)	
WHT (W)	L	L	1(0)	
W/BLK (X)	M	M	1(1)	
W/BRN (Z)	N	N	2(0)	
W/RED (R)	P	P	2(1)	
W/ORN (O)	R	R	3(0)	
W/YEL (Y)	S	S	3(1)	
W/GRN (N)	T	T	4(0)	
W/BLU (B)	U	U	MB 4(1)	
W/VIO (V)	PDØ1V	MD36V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 4)

JACK ☐ PLUG ☒ FEMALE ☐ MALE ☒	LOCATION, LENGTH, ROUTE PEØ1 & ME36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PEØ1A	ME36A	TTI 6(1)	
W/BRN (Z)	B	B	TTI 7(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	MB 5(0)	
W/YEL (Y)	E	E	5(1)	
W/GRN (N)	F	F	6(0)	
W/BLU (B)	H	H	6(1)	
W/VIO (V)	J	J	7(0)	
W/GRY (G)	K	K	7(1)	
WHT (W)	L	L	8(0)	
W/BLK (X)	M	M	8(1)	
W/BRN (Z)	N	N	9(0)	
W/RED (R)	P	P	9(1)	
W/ORN (O)	R	R	10(0)	
W/YEL (Y)	S	R	10(1)	
W/GRN (N)	T	T	11(0)	
W/BLU (B)	U	U	MB 11(1)	
W/VIO (V)	PEØ1V	ME36V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 5)

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	PFØ1 & MF36

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PFØ1A	MF36A	FETCH (F)	
W/BRN (Z)	B	B	B SET	
W/RED (R)	C	C	MEMORY STROBE ENB	
W/ORN (O)	E	E	MEM START	
W/YEL (Y)	F	F	T 1	
W/GRN (N)	H	H	T 2A	
W/BLU (B)	J	J	IOP 1	
W/VIO (V)	K	K	IOP 2	
W/GRY (G)	L	L	IOP 4	
WHT (W)	M	M	PWR CLR	
W/BLK (X)	N	N	E SET	
W/BRN (Z)	P	P	TTI AC	
W/RED (R)	R	R	SKIP	
W/ORN (O)	S	S	INTERRUPT	
W/YEL (Y)	T	T	MEM DONE	
W/GRN (N)	U	U	IOT 032	
W/BLU (B)	PFØ1V	MF36V	GND	
W/VIO (V)				

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 6)

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	PDØ2 & MD35

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PDØ2A	MD35A	JMS	
W/BRN (Z)	B	B	INT ACK	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	SR→PC	
W/YEL (Y)	E	E	MB→PC ENABLE 0-4	
W/GRN (N)	F	F	0→PC 5-11	
W/BLU (B)	H	H	OPR	
W/VIO (V)	J	J	IM 6	
W/GRY (G)	K	K	9	
WHT (W)	L	L	7	
W/BLK (X)	M	M	10	
W/BRN (Z)	N	N	8	
W/RED (R)	P	P	IM 11	
W/ORN (O)	R	R	MB→PC ENABLE 0-4	
W/YEL (Y)	S	S	MEM. EXT.	
W/GRN (N)	T	T	IOT	
W/BLU (B)	U	U	INT. INHIBIT	
W/VIO (V)	PDØ2V	MD35V	GND	

CL-A-8-0-30 Processor and Memory Chassis Connectors (Sheet 7)

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	PB 04

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PB 04	A	MQ 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)		N	MQ 11 (1)	
W/RED (R)		P	SR 6	
W/ORN (O)		R	7	
W/YEL (Y)		S	8	
W/GRN (N)		T	9	
W/BLU (B)		U	10	
W/VIO (V)	PB 04	V	SR 11	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-31 Indicator Connectors for MQ and SR Bits

JACK ☐ PLUG ☒	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE ☒	

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PB 05	A	LINK	
W/BRN (Z)	PB 05	B	RUN (1)	◆—
W/RED (R)	PB 05	C	PAUSE	
W/ORN (O)	PB 05	D	ION	
W/YEL (Y)		E		
W/GRN (N)		F		
W/BLU (B)		H		
W/VIO (V)		J		
W/GRY (G)		K		
WHT (W)		L		
W/BLK (X)		M		
W/BRN (Z)		N		
W/RED (R)	PB 05	P	SINGLE STEP	
W/ORN (O)	PB 05	R	SINGLE INST.	
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-32 Indicator Connectors for PB05

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PE 02		
W/BRN	IM 0	D			
W/RED	GND	X			
W/ORN	IM 1	E			
W/YEL	GND	F			
W/GRN	IM 2	H			
W/BLU	GND	J			
W/VIO	IM 3	K			
W/GRY	GND	L			
WHT	IM 4	M			
W/BLK	GND	N			
W/BRN	IM 5	P			
W/RED	GND	R			
W/ORN	IM 6	S			
W/YEL	GND	X			
W/GRN	IM 7	T			
W/BLU	GND	U			
W/VIO	IM 8	V			
W/GRY	GND	X	PE 02		

CL-A-8P-0-34 Input Mixer (Sheet 1)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	PF 02		
W/BRN	IM 9	D			
W/RED	G N D	X			
W/ORN	IM 10	E			
W/YEL	G N D	F			
W/GRN	IM 11	H			
W/BLU	G N D	J			
W/VIO	SKIP	K			
W/GRY	G N D	L			
WHT	INTERRUPT	M			
W/BLK	G N D	N			
W/BRN	AC CLEAR	P			
W/RED	G N D	R			
W/ORN	RUN (1)	S			
W/YEL	G N D	X			
W/GRN		T			
W/BLU	G N D	U			
W/VIO		V			
W/GRY	G N D	X	PF 02		

CL-A-8P-0-34 Input Mixer (Sheet 2)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	ME34		
W/BRN	BAC 0 (1)	D			
W/RED	G N D	X			
W/ORN	BAC 1 (1)	E			
W/YEL	G N D	F			
W/GRN	BAC 2 (1)	H			
W/BLU	G N D	J			
W/VIO	BAC 3 (1)	K			
W/GRY	G N D	L			
WHT	BAC 4 (1)	M			
W/BLK	G N D	N			
W/BRN	BAC 5 (1)	P			
W/RED	G N D	R			
W/ORN	BAC 6 (1)	S			
W/YEL	G N D	X			
W/GRN	BAC 7 (1)	T			
W/BLU	G N D	U			
W/VIO	BAC 8 (1)	V			
W/GRY	G N D	X	ME34		

CL-A-8M-0-35 AC Bits and IOP's (Sheet 1)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	MF34		
W/BRN	BAC 9 (1)	D			
W/RED	G N D	X			
W/ORN	BAC 10 (1)	E			
W/YEL	G N D	F			
W/GRN	BAC 11 (1)	H			
W/BLU	G N D	J			
W/VIO	IOP 1	K			
W/GRY	G N D	L			
WHT	IOP 2	M			
W/BLK	G N D	N			
W/BRN	IOP 4	P			
W/RED	G N D	R			
W/ORN	T 1	S			
W/YEL	G N D	X			
W/GRN	T 2	T			
W/BLU	G N D	U			
W/VIO	PWR CLR	V			
W/GRY	G N D	X	MF34		

CL-A-8M-0-35 AC Bits and IOP's (Sheet 2)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	PE 03		
W/BRN	DATA ADD 0	D			
W/RED	G N D				
W/ORN	DATA ADD 1	E			
W/YEL	G N D	F			
W/GRN	DATA ADD 2	H			
W/BLU	G N D	J			
W/VIO	DATA ADD 3	K			
W/GRY	G N D	L			
WHT	DATA ADD 4	M			
W/BLK	G N D	N			
W/BRN	DATA ADD 5	P			
W/RED	G N D	R			
W/ORN	DATA ADD 6	S			
W/YEL	G N D				
W/GRN	DATA ADD 7	T			
W/BLU	G N D	U			
W/VIO	DATA ADD 8	V			
W/GRY	G N D		PE 03		

CL-A-8P-0-36 Data Address (Sheet 1)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	PF 03		
W/BRN	DATA ADD 9	D			
W/RED	G N D	X			
W/ORN	DATA ADD 10	E			
W/YEL	G N D	F			
W/GRN	DATA ADD 11	H			
W/BLU	G N D	J			
W/VIO	BRK. REQUEST	K			
W/GRY	G N D	L			
WHT	DATA DIRCT.	M			
W/BLK	G N D	N			
W/BRN	BREAK (B)	P			
W/RED	G N D	R			
W/ORN	ADD ACCEPTED	S			
W/YEL	G N D	X			
W/GRN	MB INCREMENT	T			
W/BLU	G N D	U			
W/VIO		V			
W/GRY	G N D	X	PF 03		

CL-A-8P-0-36 Data Address (Sheet 2)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PE 04		
W/BRN	MB 0 IN	D			
W/RED	GND	X			
W/ORN	MB 1 IN	E			
W/YEL	GND	F			
W/GRN	MB 2 IN	H			
W/BLU	GND	J			
W/VIO	MB 3 IN	K			
W/GRY	GND	L			
WHT	MB 4 IN	M			
W/BLK	GND	N			
W/BRN	MB 5 IN	P			
W/RED	GND	R			
W/ORN	MB 6 IN	S			
W/YEL	GND	X			
W/GRN	MB 7 IN	T			
W/BLU	GND	U			
W/VIO	MB 8 IN	V			
W/GRY	GND	X	PE 04		

CL-A-8P-0-37 MB's In (Sheet 1)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PF 04		
W/BRN	MB 9 IN	D			
W/RED	GND	X			
W/ORN	MB 10 IN	E			
W/YEL	GND	F			
W/GRN	MB 11 IN	H	PF 04		
W/BLU	GND	J			
W/VIO	CYCLE SELECT	K	PF 04		
W/GRY	GND	L			
WHT	+1→CA INH.	M	PF 04		
W/BLK	GND	N			
W/BRN	WC OVERFLOW	P	PF 04		
W/RED	GND	R			
W/ORN		S			
W/YEL	GND	X			
W/GRN		T			
W/BLU	GND	U			
W/VIO		V			
W/GRY	GND	X			

CL-A-8P-0-37 MB's In (Sheet 2)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	ME35		
W/BRN	BMB 0 (1)	D			
W/RED	GND	X			
W/ORN	BMB 1 (1)	E			
W/YEL	GND	F			
W/GRN	BMB 2 (1)	H			
W/BLU	GND	J			
W/VIO	BMB 3 (0)	K			
W/GRY	GND	L			
WHT	BMB 3 (1)	M			
W/BLK	GND	N			
W/BRN	BMB 4 (0)	P			
W/RED	GND	R			
W/ORN	BMB 4 (1)	S			
W/YEL	GND	X			
W/GRN	BMB 5 (0)	T			
W/BLU	GND	U			
W/VIO	BMB 5 (1)	V			
W/GRY	GND	X	ME35		

CL-A-8M-0-38 MB Bits (Sheet 1)

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	MF35		
W/BRN	BMB 6 (0)	D			
W/RED	G N D				
W/ORN	BMB 6 (1)	E			
W/YEL	G N D	F			
W/GRN	BMB 7 (0)	H			
W/BLU	G N D	J			
W/VIO	BMB 7 (1)	K			
W/GRY	G N D	L			
WHT	BMB 8 (0)	M			
W/BLK	G N D	N			
W/BRN	BMB 8 (1)	P			
W/RED	G N D	R			
W/ORN	BMB 9 (1)	S			
W/YEL	G N D				
W/GRN	BMB 10 (1)	T			
W/BLU	G N D	U			
W/VIO	BMB 11 (1)	V			
W/GRY	G N D		MF35		

CL-A-8M-0-38 MB Bits (Sheet 2)

JACK ☐ PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE ☐ MALE [X]	MA 35

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	MA 35	A	DATA FIELD 0	
W/BRN (Z)		B	DATA FIELD 1	
W/RED (R)		C	DATA FIELD 2	
W/ORN (O)		D	INST FIELD 0	
W/YEL (Y)		E	INST FIELD 1	
W/GRN (N)		F	INST FIELD 2	
W/BLU (B)		H		
W/VIO (V)		J		
W/GRY (G)		K		
WHT (W)		L		
W/BLK (X)		M		
W/BRN (Z)		N		
W/RED (R)		P	DATA FIELD SR 0	
W/ORN (O)		R	DATA FIELD SR 1	
W/YEL (Y)		S	DATA FIELD SR 2	
W/GRN (N)		T	INST FIELD SR 0	
W/BLU (B)		U	INST FIELD SR 1	
W/VIO (V)	MA 35	V	INST FIELD SR 2	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8M-0-39 Indicator Connector MA-35

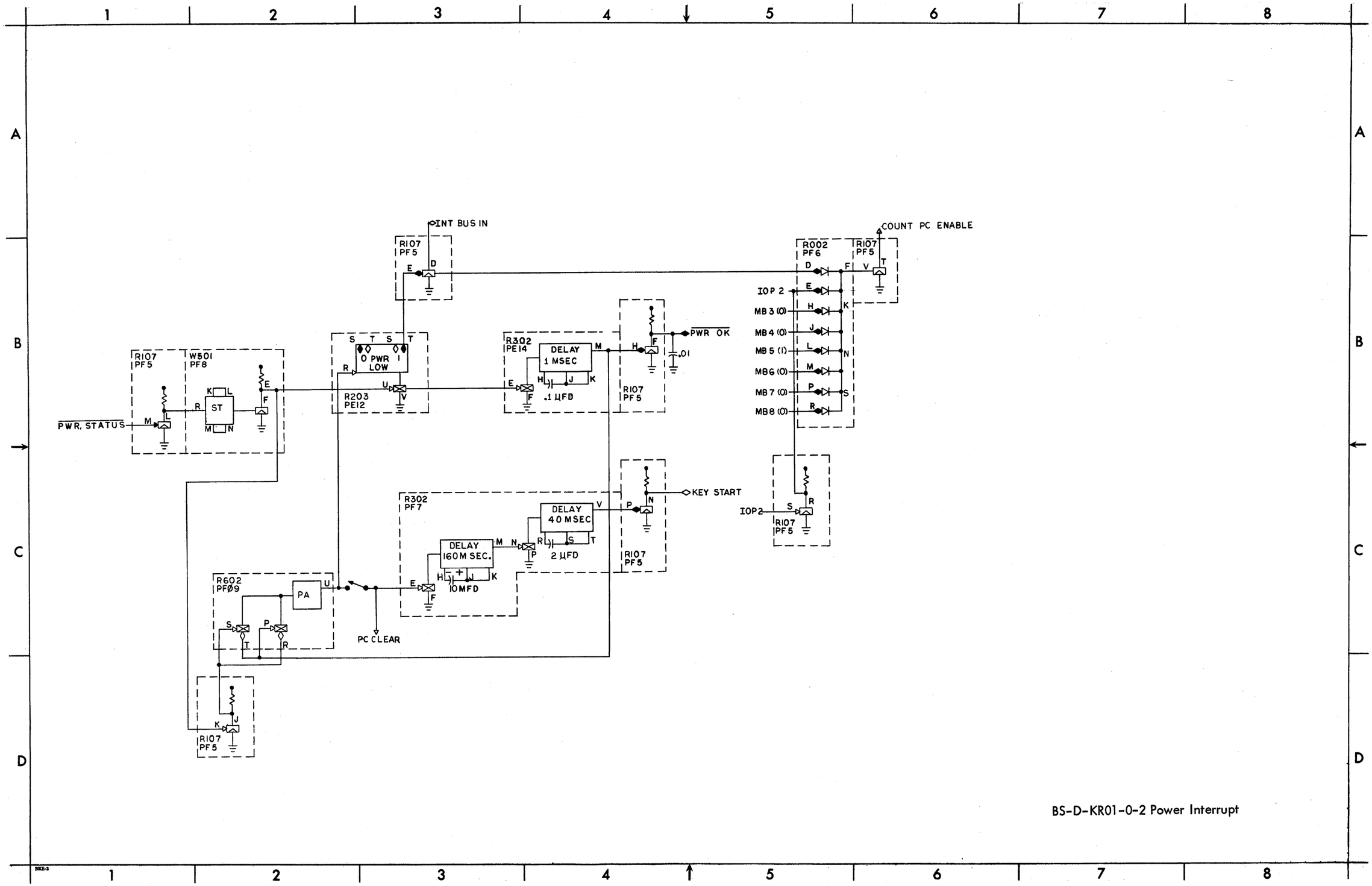
COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	ME 31		
W/BRN	SA P	D			
W/RED	GND	X			
W/ORN	SA 0	E			
W/YEL	GND	F			
W/GRN	SA 1	H			
W/BLU	GND	J			
W/VIO	SA 2	K			
W/GRY	GND	L			
WHT	SA 3	M			
W/BLK	GND	N			
W/BRN	SA 4	P			
W/RED	GND	R			
W/ORN	SA 5	S			
W/YEL	GND	X			
W/GRN	SA 6	T			
W/BLU	GND	U			
W/VIO	SA 7	V			
W/GRY	GND	X	ME 31		

CL-A-8M-0-40 Sense Amplifiers (Sheet 1)

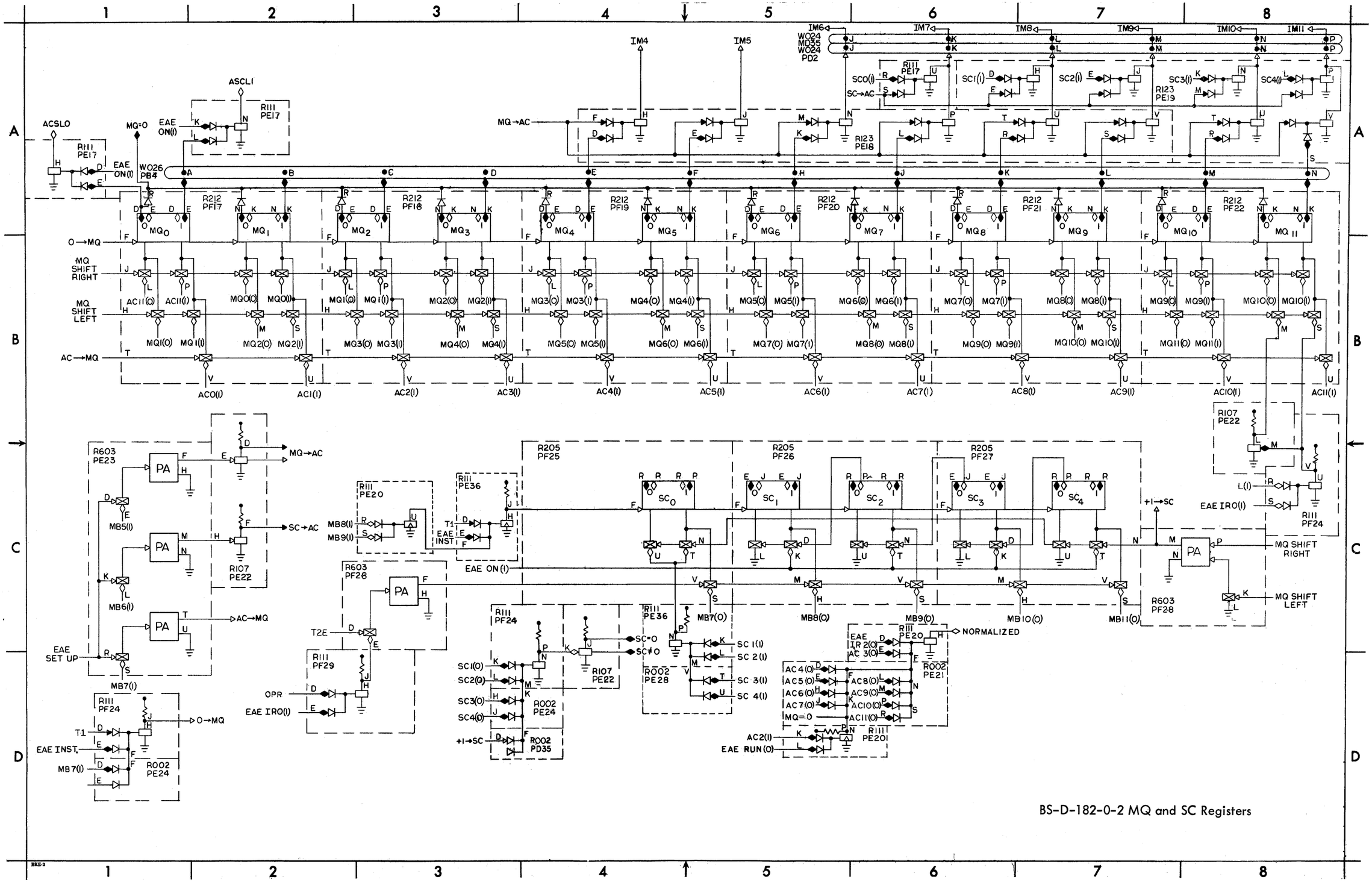
COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	G N D	C	MF 31		
W/BRN	SA 8	D			
W/RED	G N D	X			
W/ORN	SA 9	E			
W/YEL	G N D	F			
W/GRN	SA 10	H			
W/BLU	G N D	J			
W/VIO	SA 11	K			
W/GRY	G N D	L			
WHT	PWR CLR	M			
W/BLK	G N D	N			
W/BRN		P			
W/RED	G N D	R			
W/ORN		S			
W/YEL	G N D	X			
W/GRN		T			
W/BLU	G N D	U			
W/VIO		V			
W/GRY	G N D	X	MF 31		

CL-A-8M-0-40 Sense Amplifiers (Sheet 2)

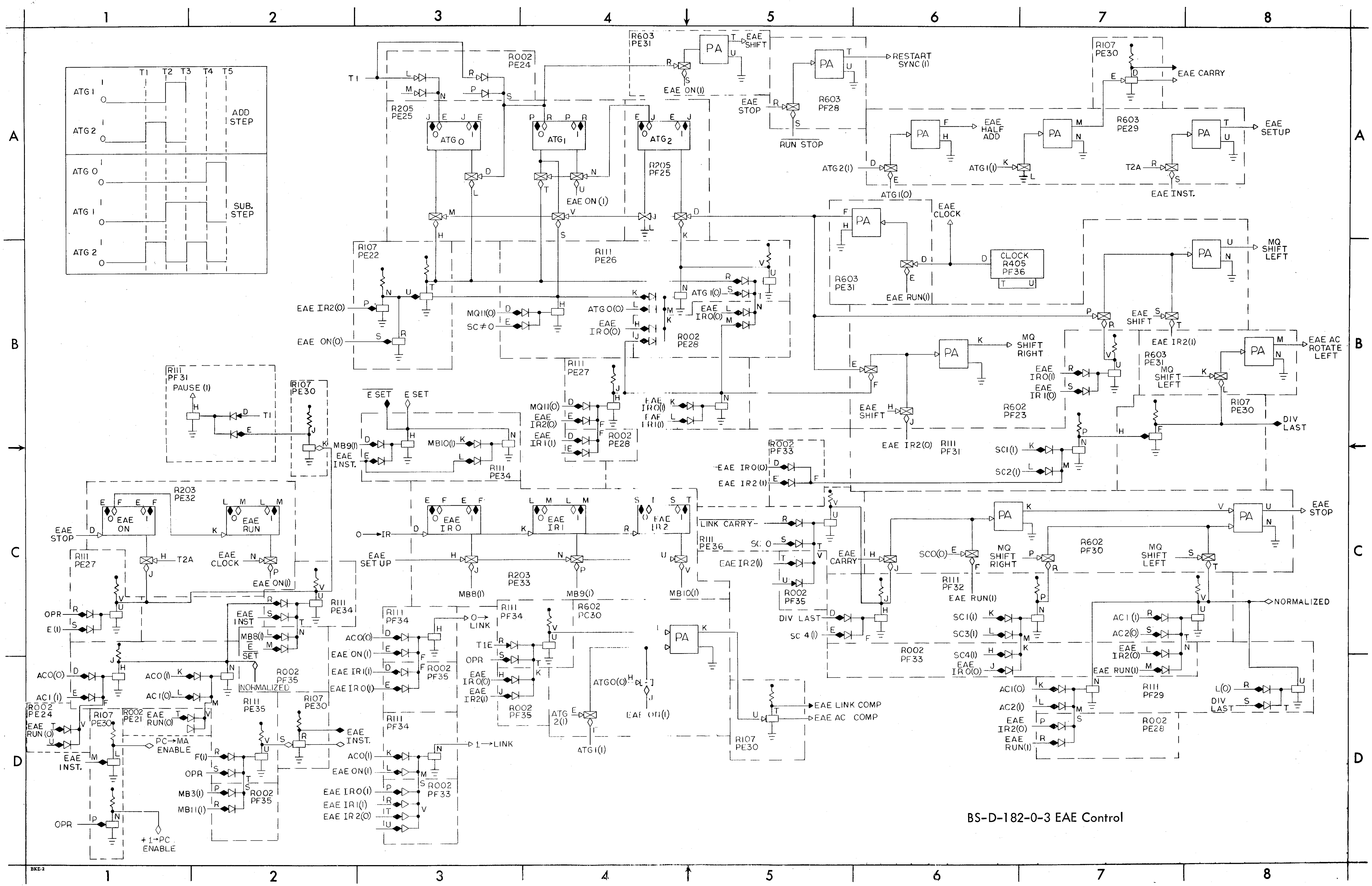
COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
	+10V	A	MF30		BLANK
	-15V	B			BLANK
W/BLK	G N D	C			
W/BRN	KEY BOARD GENERATOR	D			
W/RED	G N D	X			
W/ORN		E			
W/YEL	G N D	F			
W/GRN	SELECTOR MAGNETS	H			
W/BLU	G N D	J			
W/VIO		K			
W/GRY	G N D	L			
WHT	POWER SWITCHES	M			
W/BLK	G N D	N			
W/BRN		P			
W/RED	G N D	R			
W/ORN		S			
W/YEL	G N D	X			
W/GRN		T			
W/BLU	G N D	U			
W/VIO		V			
W/GRY	G N D	X	MF30		



BS-D-KR01-0-2 Power Interrupt

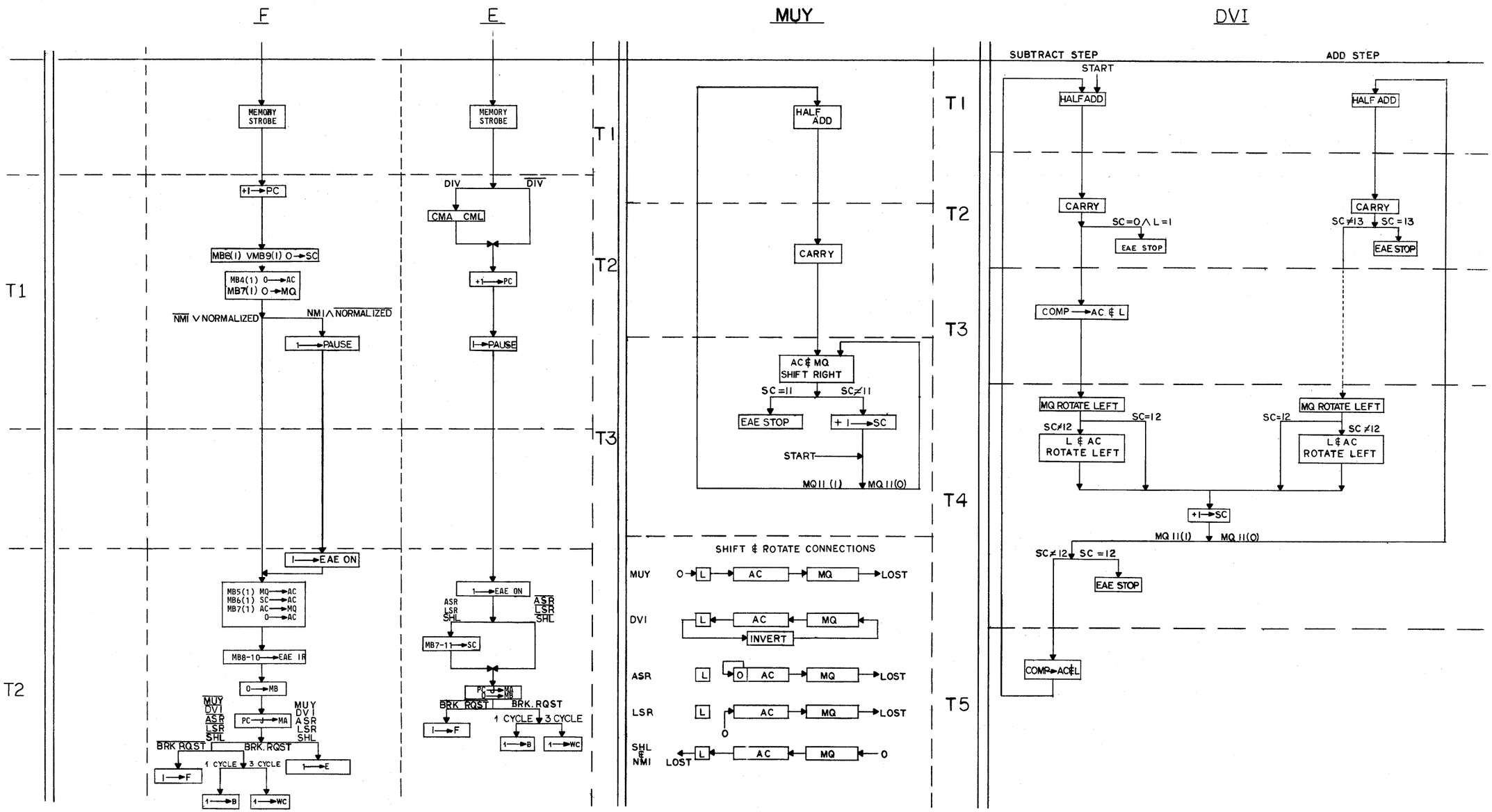


BS-D-182-0-2 MQ and SC Registers



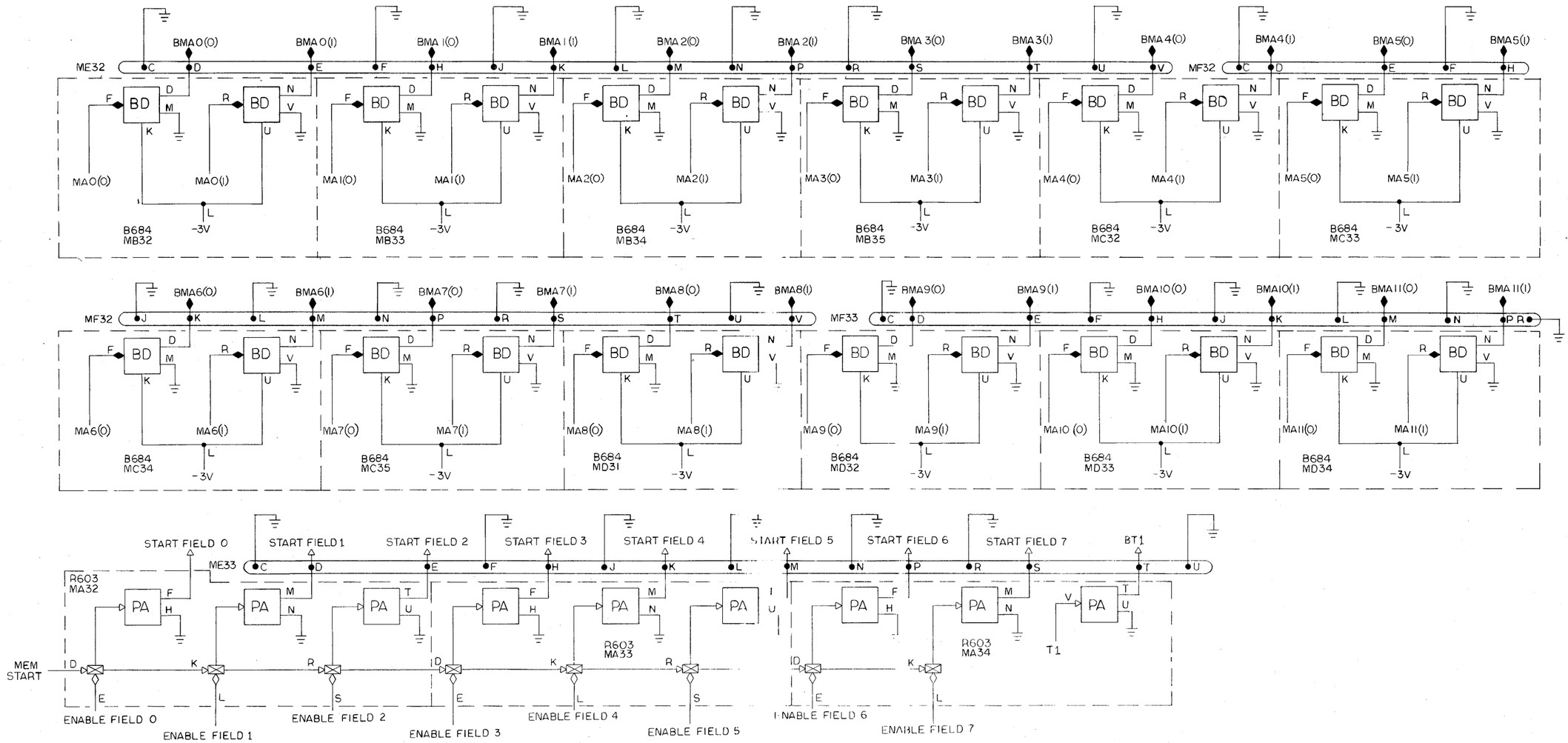
BS-D-182-0-3 EAE Control

FD-D-182-0-4 EAE Flow Diagram



FD-D-182-0-4 EAE Flow Diagram

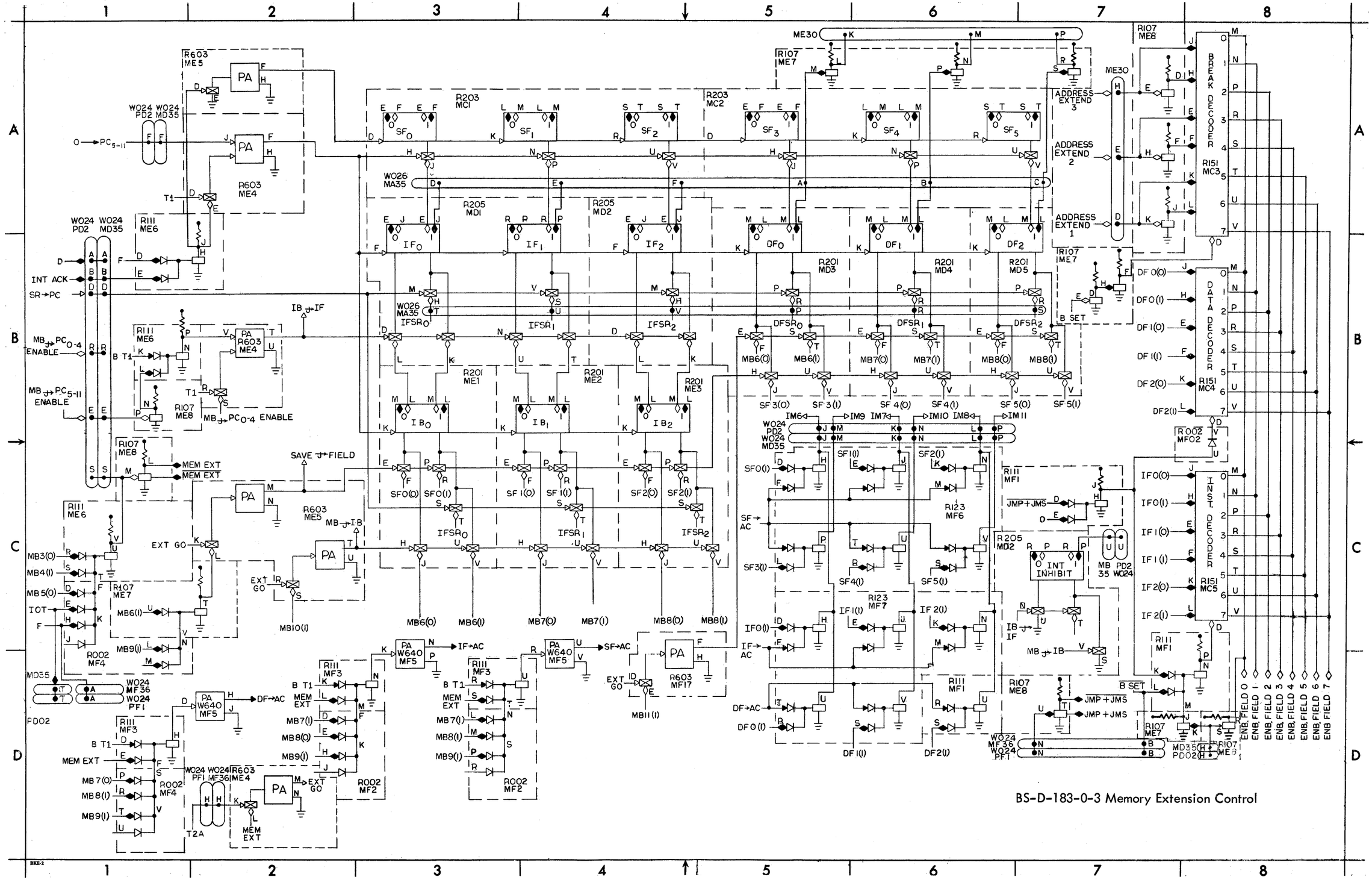
BS-D-183-0-2 MA Buffers and Start Field



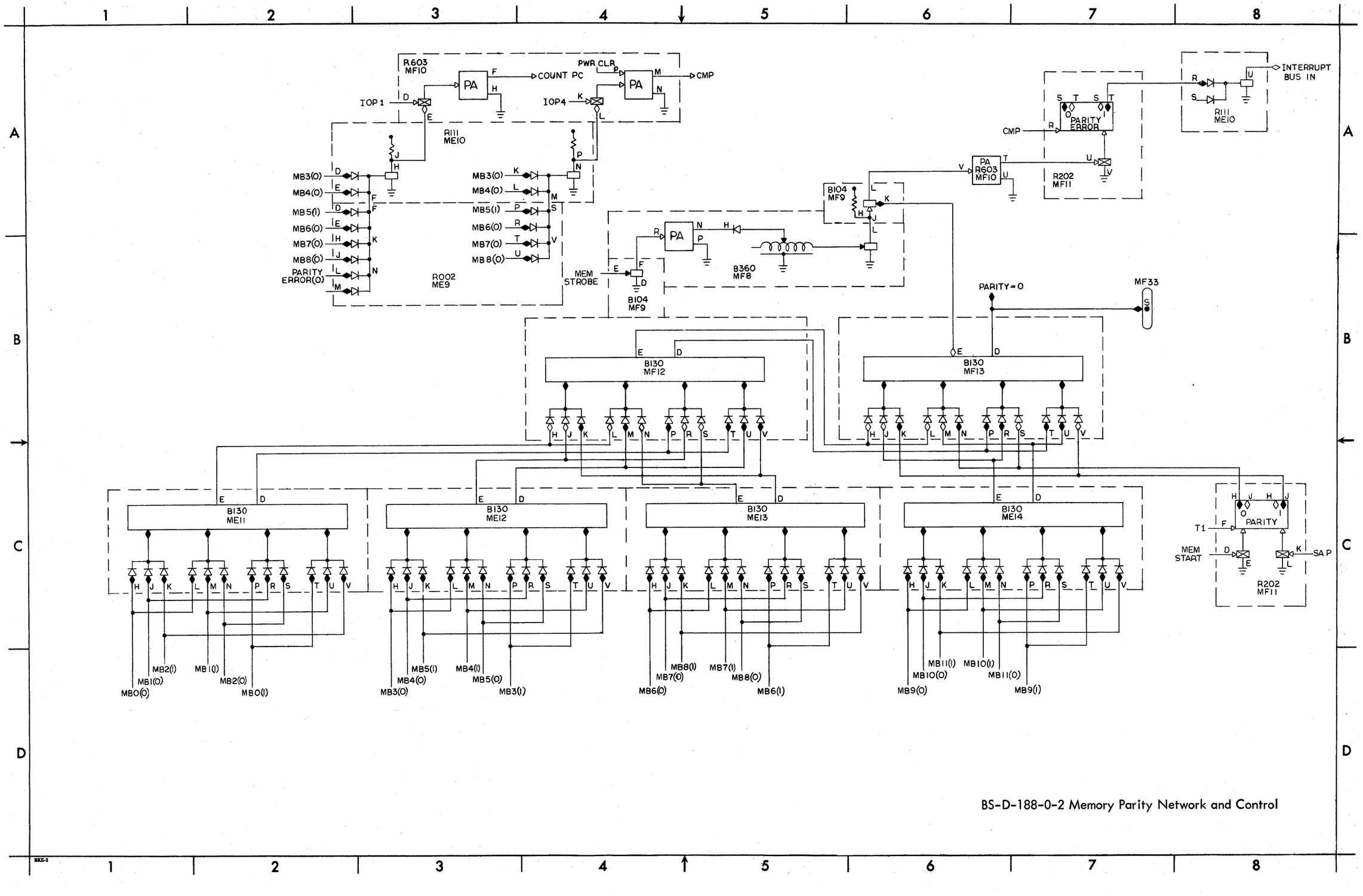
BS-D-183-0-2 MA Buffers and Start Field

BKE-2

BS-D-183-0-3 Memory Extension Control

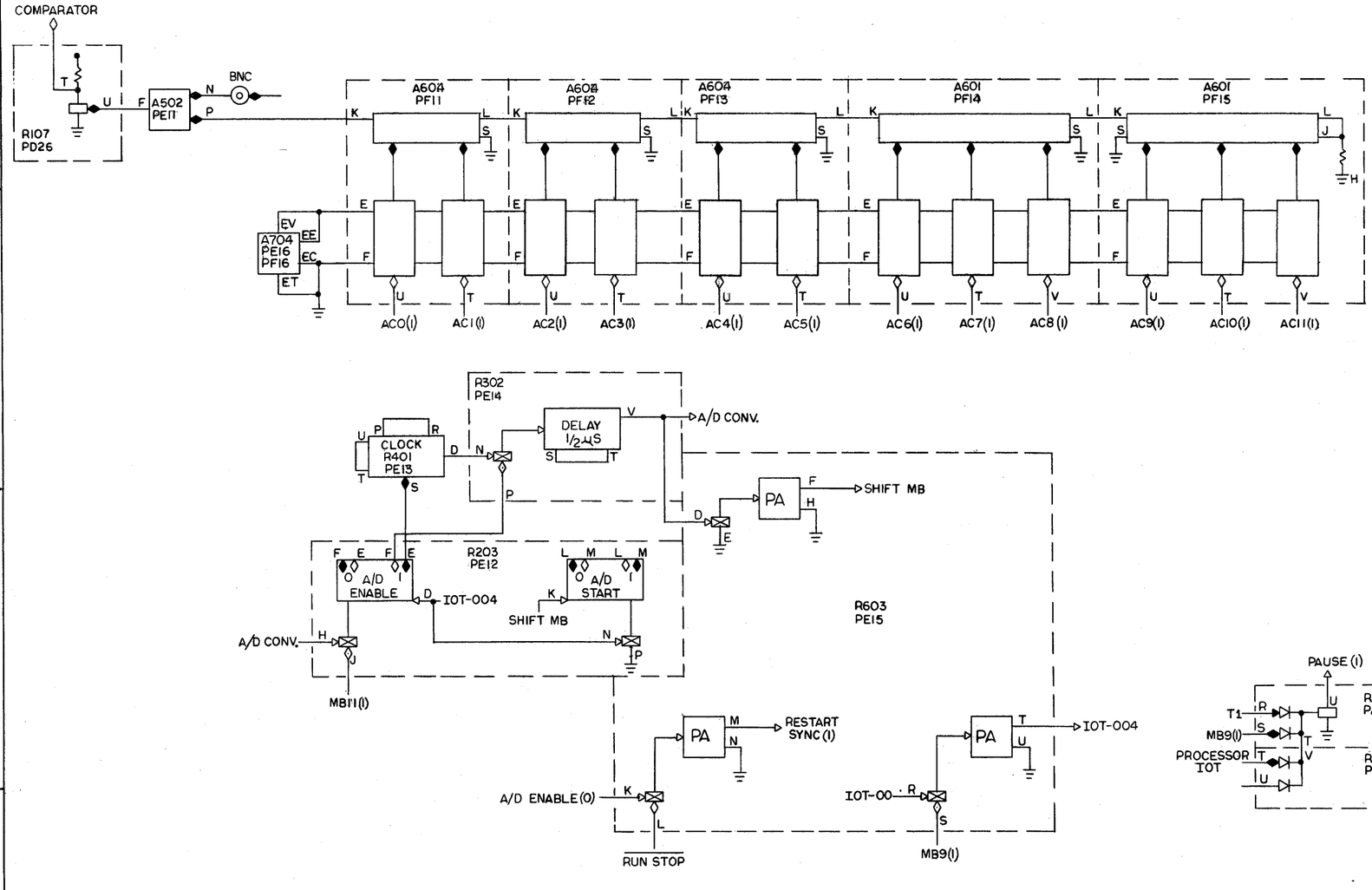


BS-D-183-0-3 Memory Extension Control

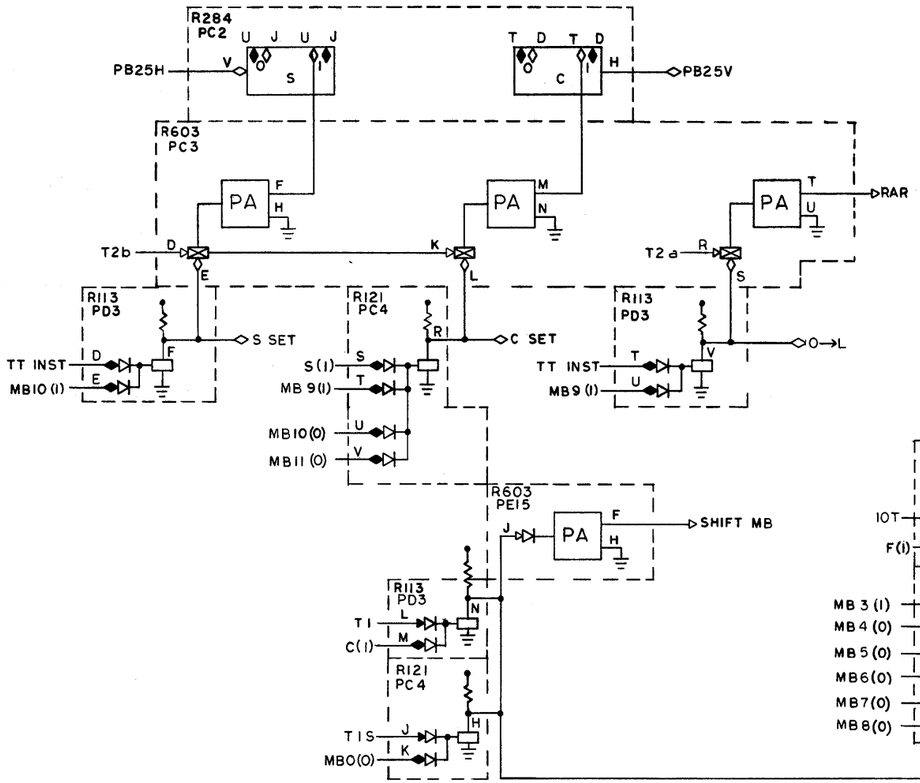


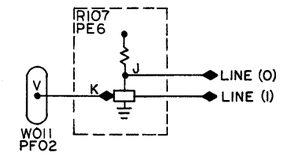
BS-D-188-0-2 Memory Parity Network and Control

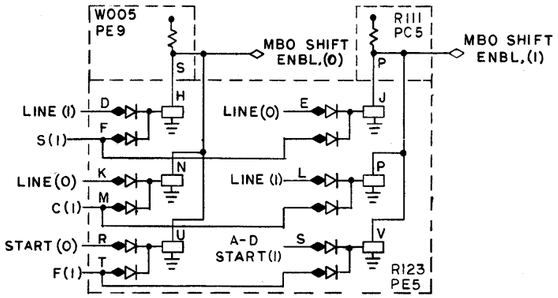
BKE-2

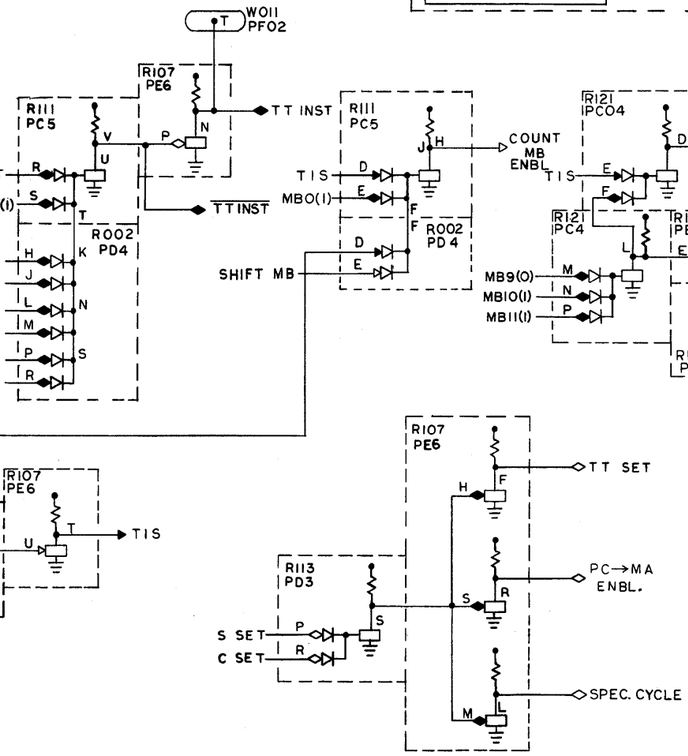


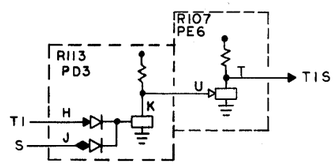
BS-D-189-0-2 A/D Converter







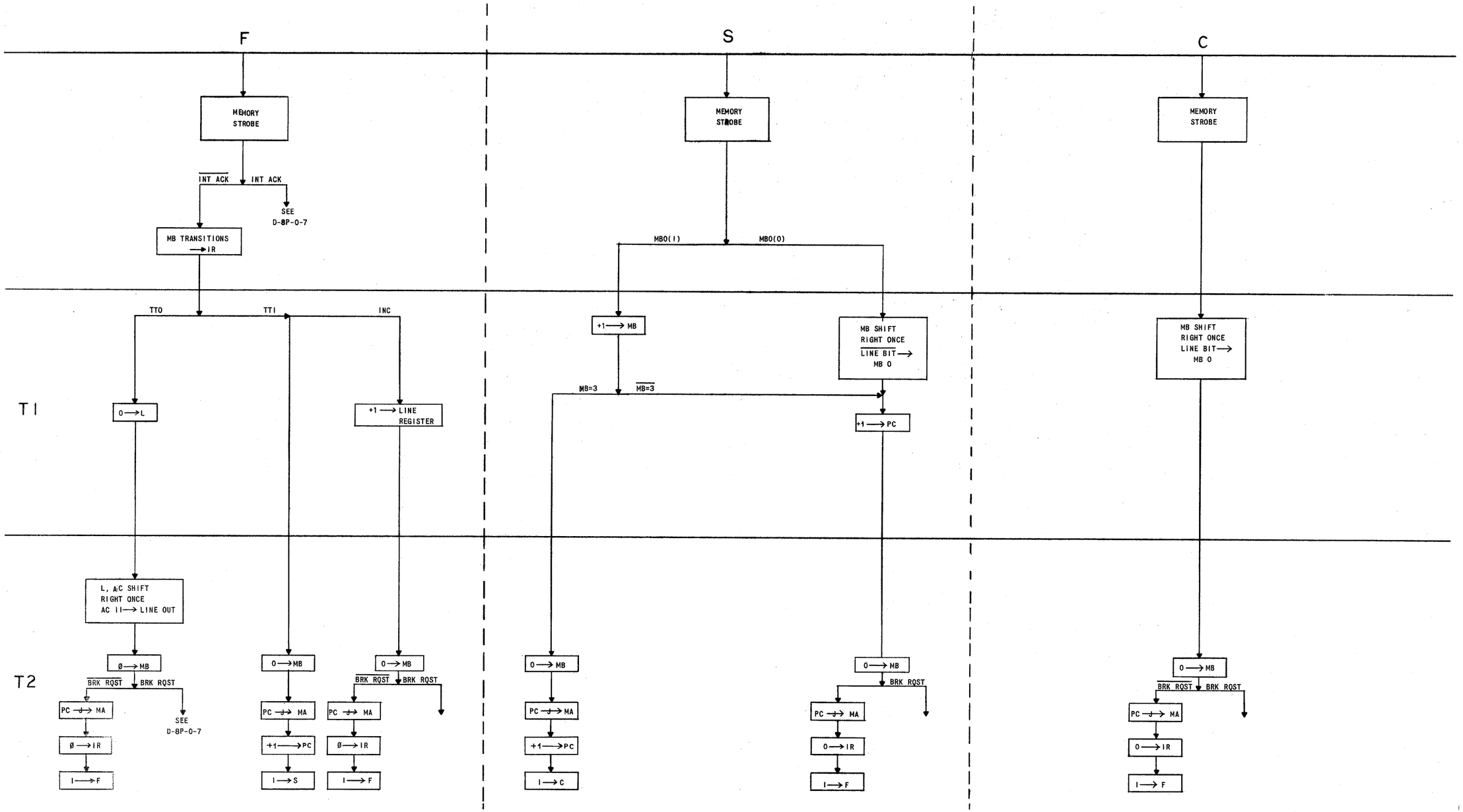




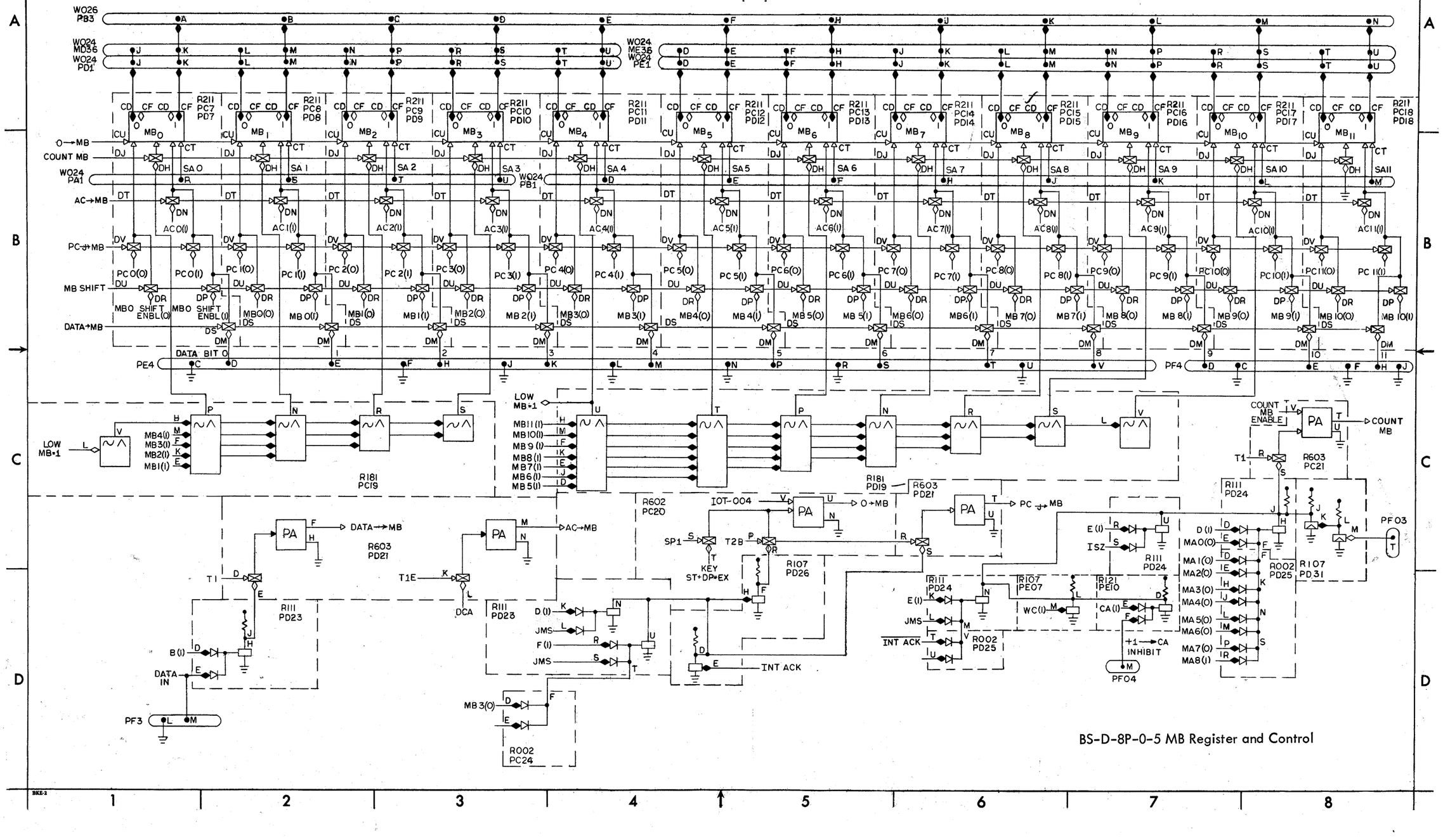
BS-D-681-0-2 Data Line Interface

BKE-2

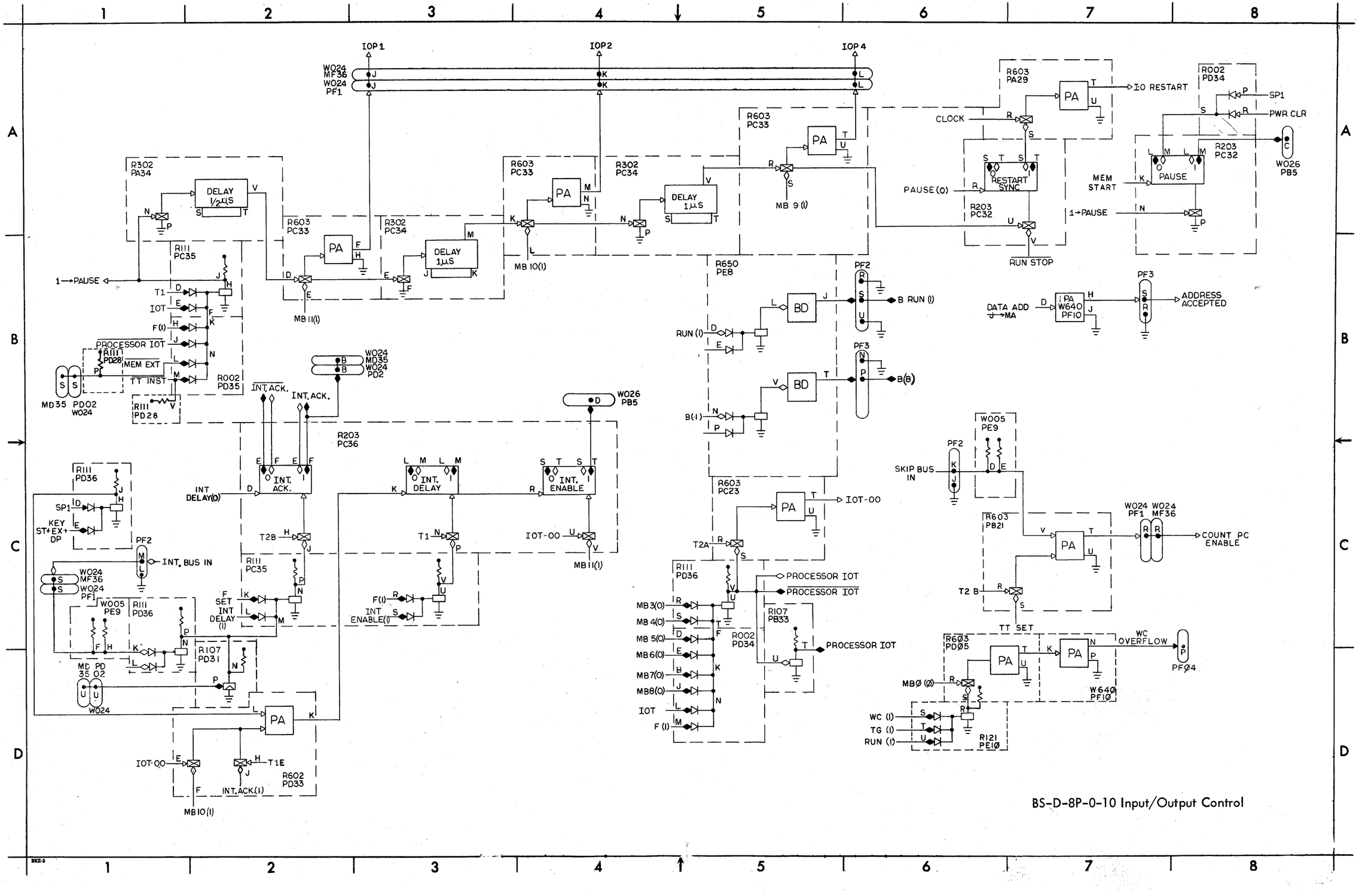
FD-D-681-0-3 Data Line Interface Flow Diagram



FD-D-681-0-3 Data Line Interface Flow Diagram



BS-D-8P-0-5 MB Register and Control



BS-D-8P-0-10 Input/Output Control

BKE-2

APPENDIX 1

SIGNAL ORIGINS

A list of the signals in the PDP-8 and the engineering drawings on which they can be found appear in Table A1-1. This information should simplify and accelerate any detailed study of the machine logic on the engineering drawings.

TABLE A1-1 SIGNAL ORIGINS

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
AC ⟶ MB	D-8P-0-5	COMP ⟶ LINK	D-8P-0-3
ACSL0, ASCL1	D-8P-0-2	COUNT MB	D-8P-0-5
AC0(0) through AC11(1)	D-8P-0-2	COUNT MB ENABLE	D-681-0-2
A/D CONV.	D-189-0-2	COUNT PC	D-8P-0-8 D-8P-0-10 D-8M-0-11
ADDRESS ACCEPTED	D-8P-0-10		
A/D START(0), A/D START(1)	D-189-0-2	COUNT PC ENABLE	D-KR01-0-2
AND, $\overline{\text{AND}}$	D-8P-0-6	D	D-8P-0-6
B	D-8P-0-6	DATA ⟶ MB	D-8P-0-5
BAC0(1) through BAC11(1)	D-8M-0-16	DATA ADD ⟶ MA	D-8P-0-8
		DCA, $\overline{\text{DCA}}$	D-8P-0-6
B(B)	D-8P-0-10	$\overline{\text{D SET}}$	D-8P-0-6
BMB0(1) through BMB11(1)	D-8M-0-16	E(1)	D-8P-0-6
		EAE AC ROTATE LEFT	D-182-0-3
B POWER CLEAR	D-8M-0-16	EAE AC COMP	D-182-0-3
B RUN(1)	D-8P-0-10	EAE LINK COMP	D-182-0-3
B SET, $\overline{\text{B SET}}$	D-8P-0-6	ENB(0), ENB(1)	D-8M-0-11
BT1	D-8M-0-16	$\overline{\text{E SET}}$	D-8P-0-6
BT2A	D-8M-0-16	F	D-8P-0-6
CA	D-8P-0-6	F SET, $\overline{\text{F SET}}$	D-8P-0-6
CARRY	D-8P-0-3	HALF ADD	D-8P-0-3
CLOCK	D-8P-0-9	INHIBIT(1)	D-8M-0-15
COMPARATOR	D-189-0-2	INT. ACK., $\overline{\text{INT. ACK.}}$	D-8P-0-10
COMP ⟶ AC	D-8P-0-3		
		INT. DELAY (1)	D-8P-0-19

TABLE A1-1 SIGNAL ORIGINS (continued)

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
INT. ENABLE(1)	D-8P-0-10	MB0(0) through MB11(1)	D-8P-0-5
INTERRUPT BUS IN	D-8M-0-11	MB0 SHIFT ENBL	D-681-0-2
INTERRUPT INHIBIT	D-183-0-3	$MB_{5-11} \xrightarrow{J} PC$	D-8P-0-8
IOP1, IOP2, IOP4	D-8P-0-10 D-8M-0-16	MB SHIFT	D-189-0-2, D-681-0-2
IO RESTART	D-8P-0-10	MEM DONE	D-8M-0-15
IOT, $\overline{IOT}$	D-8P-0-6	MEM ENABLE(1)	D-8M-0-15
$\overline{IOT + OPR}$	D-8P-0-6	MEM START	D-8P-0-9
IOT 00	D-8P-0-10	MEM STROBE	D-8M-0-15
IOT 004	D-189-0-2	MEM STROBE ENABLE	D-8P-0-9
IR0(0) through IR2(1)	D-8P-0-6	MQ SHIFT RIGHT	D-182-0-3
IS2, $\overline{IS2}$	D-8P-0-6	OPR, $\overline{OPR}$	D-8P-0-6
JMP, $\overline{JMP}$	D-8P-0-6	OP SKIP, $\overline{OP\ SKIP}$	D-8P-0-8
JMP + JMS	D-8P-0-8	OP1, OP2	D-8P-0-3
JMS, $\overline{JMS}$	D-8P-0-6	PARITY = 0	D-188-0-2
KCC IOT 032	D-8M-0-11	PAUSE(0), PAUSE(1)	D-8P-0-10 D-189-0-2
KEYBOARD FLAG(1)	D-8M-0-11		
KEYBOARD SELECT	D-8M-0-11	PB25H, PB25V	D-8P-0-6
KEY EX + DP	D-8P-0-9	PC2H, PC2V	D-681-0-2
$\overline{KEY\ LOAD\ ADDRESS}$	D-8P-0-9	PC CARRY	D-8P-0-8
KEY START	D-8P-0-9	PC CLEAR	D-KR01-0-2
KEY ST + EX + DP	D-8P-0-9	$PC \xrightarrow{J} MA$	D-8P-0-8
KRS IOT 034	D-8M-0-11	$PC \longrightarrow MA$ ENABLE	D-681-0-2
L(0), L(1)	D-8P-0-2	$PC \xrightarrow{J} MB$	D-8P-0-5
LSR0, LSR1	D-8P-0-2	PC(0) through PC11(1)	D-8P-0-4
MA0(0) through MA11(1)	D-8P-0-4	POP1	D-8P-0-3
$MB \xrightarrow{0} AC$	D-8P-0-3	PROCESSOR IOT, $\overline{PROCESSOR\ IOT}$	D-8P-0-10
$MB \xrightarrow{J} MA_{0-4}$	D-8P-0-8	PWR CLR	D-8P-0-9
$MB \xrightarrow{J} MA_{5-11}$	D-8P-0-8	$\overline{PWR\ OK}$	D-8P-0-9
$MB \xrightarrow{J} PC_{0-4}$	D-8P-0-8	RAL	D-8P-0-3
$MB \xrightarrow{J} PC_{0-4}$ ENABLE	D-8P-0-8	RAR	D-8P-0-3
$MB \xrightarrow{J} PC_{5-11}$ ENABLE	D-8P-0-8	READ(1)	D-8M-0-15

TABLE A1-1 SIGNAL ORIGINS (continued)

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
RESTART SYNC(1)	D-189-0-2	$\overline{\text{TT INST}}$	D-681-0-2
RTR	D-8P-0-3	TTI0(0) through TTI7(1)	D-8M-0-11
RUN STOP, $\overline{\text{RUN STOP}}$	D-8P-0-9	TT0 CLOCK	D-8M-0-11
RUN(0), RUN(1)	D-8P-0-9	TT0(0) through TT07(1)	D-8M-0-11
SA P	D-8M-0-15	TT0=0	D-8M-0-11
SA0 through SA11	D-8M-0-15	T1, T1E	D-8P-0-9
SHIFT MB	D-189-0-2	T2A, T2B, T2E	D-8P-0-9
SP STOP	D-8P-0-9	WC(1)	D-8P-0-6
SP0, SP1, SP2, SP3	D-8P-0-9	WC + WC SET	D-8P-0-6
SR ⟶ AC	D-8P-0-3	WRITE(1)	D-8M-0-15
SR ⟶ PC	D-8P-0-8	0 ⟶ AC	D-8P-0-3
STOP(0), STOP(1)	D-8M-0-11	0 ⟶ L	D-8P-0-3
TAD, $\overline{\text{TAD}}$	D-8P-0-6	0 ⟶ MA_{0-4}	D-8P-0-8
TCF IOT 042	D-8M-0-11	0 ⟶ MA_{5-11}	D-8P-0-8
TELEPRINTER FLAG(1)	D-8M-0-11	0 ⟶ MB	D-8P-0-5
TELEPRINTER SELECT	D-8M-0-11	0 ⟶ PC_{0-4}	D-8P-0-8
TPC IOT 044	D-8M-0-11	0 ⟶ PC_{5-11}	D-8P-0-8
TTI ⟶ AC	D-8M-0-11	1 ⟶ L	D-8P-0-3, D-182-0-3
TTI CLOCK	D-8M-0-11		
		+1 ⟶ PC ENABLE	D-8P-0-8

APPENDIX 2

DIGITAL PROGRAM LIBRARY

The following is a current list of program tapes and descriptive material for programs applicable to the PDP-8. DEC constantly develops, field tests, and documents into the Digital Program Library new techniques, routines, and programs for incorporation into users' systems.

SYSTEM PROGRAMS

Digital	8-1-S	Symbolic Editor
Digital	8-1-SL	Symbolic Editor Listing
Digital	8-2-S	FORTRAN System
Digital	8-2-SL	FORTRAN Operating System Listing
Digital	8-3-S	PAL III (Program Assembler Language)
Digital	8-3-SL	PAL III Listing
Digital	8-4-S	DDT-8
Digital	8-5-S	Floating-Point System
Digital	8-6-S	Symbol Print
Digital	8-7-S	DECtape Library System
Digital	8-8-S	MACRO 8
Digital	8-9-S	DECtape FORTRAN
Digital	8-10-S	CALCULATOR System
Digital	8-11-S	DATAK System (Data Acquisition Program)
Digital	8-12-S	ODT-8
Digital	8-13/14-S	Multianalyzer Programs
Digital	8-15-S	Oceanographic Analysis
Digital	8-16-S	Master Tape Duplicator
Digital	8-35-S-A	TTY 680 5-Bit Character Assembly Subroutines
Digital	8-35-S-B	TTY 680 8-Bit Character Assembly Subroutines

ELEMENTARY FUNCTION ROUTINES

Digital	8-9-F	Square Root Subroutine - Single Precision
Digital	8-11-F	Signed Multiply Subroutine - Single Precision
Digital	8-12-F	Signed Divide Subroutine - Single Precision
Digital	8-13-F	Double-Precision Multiply Subroutine - Signed
Digital	8-14-F	Double-Precision Divide Subroutine - Signed
Digital	8-15-F	Sine Routine - Single Precision
Digital	8-16-F	Sine Routine - Double Precision
Digital	8-17-F	Cosine Routine - Single Precision
Digital	8-18-F	Sine Routine - Double Precision
Digital	8-20-F	Four Word Floating Point Package
Digital	8-21-F	Signed Multiply Single Precision Using EAE Type 182
Digital	8-22-F	Signed Divide Single Precision Using EAE Type 182
Digital	8-23-F	Signed Multiply Double Precision Using EAE Type 182
Digital	8-25-F	Floating Point Package EAE

UTILITY PROGRAMS

Digital	8-0	Format for PDP-8 Program Documentation
Digital	8-1-U	Read-In-Mode Loader
Digital	8-2-U-Rim	Binary Loader (ASR-33 or 750C)
Digital	8-2A-U-Rim	Binary Loader (Extended Memory, ASR-33)
Digital	8-2B-U-Rim	Binary Loader (Extended Memory, 750C)
Digital	8-3-U	DECtape Library System Loader
Digital	8-4-U-Rim	Read-In-Mode Punch ASR-33
Digital	8-5-U-Sym	Binary Punch 33/75E
Digital	8-6-U-Sym	Octal Memory Dump
Digital	8-7-U-Sym	Logical Subroutines
Digital	8-8-U-Sym	Arithmetic Shift Subroutines
Digital	8-9-U-Sym	Logical Shift Subroutines
Digital	8-12-U	Incremental Plotter Subroutines
Digital	8-14-U-Sym	Binary to Binary-Coded-Decimal Conversion
Digital	8-15-U	Binary to Binary-Coded-Decimal Conversion (Four Digit)
Digital	8-16-U-Sym	Binary to Binary-Coded-Decimal Conversion (Compatible with IBM BCD Mode Mag-Tape Format)
Digital	8-17-U	EAE Instruction Set Simulator
Digital	8-18-U-Sym	Subroutine for Alphanumeric Message Typeout
Digital	8-19-U-Sym	Teletype Output Subroutines
Digital	8-20-U	Character String Typeout
Digital	8-21-U-Sym	Symbolic Tape Format Generator
Digital	8-22-U	Unsigned Decimal Print
Digital	8-26-U-Bin	DECTOG
Digital	8-27-U-Bin	DECtape Subroutines
Digital	8-28-U	580 Tape Control Subroutines
Digital	8-32-U	Binary Punch (6 Channel)
Digital	8-33-U	5/8 TOG
Digital	8-34-U	DECEX DECtape Exerciser

APPLICATION PROGRAMS

Application Note 801	Scaling for Fixed-Point, 2's Complement Arithmetic
Application Note 802	Matrix Inversion
Application Note 803	Performance Capability Program (Edit Subprogram)
Application Note 804	Throughput to IBM-Compatible Magnetic Tape
Application Note 805	Linearization Subprogram

MAINTENANCE PROGRAMS

A complete collection of maintenance and diagnostic programs is available for the basic computer and many of its options. Table 9-1 lists these Maindec programs for the basic PDP-8.

DECUS LIBRARY

DECUS No. 5-1	Binary Package
DECUS No. 5-2	Octal Package and Symbolic Dump
DECUS No. 5-3	BRL - A Binary Relocatable Loader with Transfer Vector Options for the PDP-5 Computer
DECUS No. 5-4	Octal Typeout of Memory Area with Format Option
DECUS No. 5-5	Expanded Adding Machine
DECUS No. 5-6	BCD-to-Binary Conversion of 3-Digit Numbers
DECUS No. 5/8-7	Decimal-to-Binary Conversion by Radix Deflation on PDP-8
DECUS No. 5-8	PDP-5 Floating Point Routines
DECUS No. 5/8-9	Analysis of Variance PDP-5/8
DECUS No. 5-10	Paper Tape Reader Tester
DECUS No. 5-11	PDP-5 Debug System
DECUS No. 5-12	Pack-Punch Processor and Reader for the PDP-5
DECUS No. 5-13	PDP-5 Assembler
DECUS No. 5-14	Dice Game for the PDP-5
DECUS No. 5-15	ATEPO (Auto Test in Elementary Programming and Operation of a PDP-5 Computer)
DECUS No. 5-16	Tape Duplicator for PDP-5/8
DECUS No. 5-17	Type 250 Drum Transfer Routine for Use on PDP-5/8